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Design and Analysis of an 8-Bit Parallel-In Parallel-Out Register Using an 18-Transistor Hybrid Flip-Flop for Low-Power Applications

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Abstract—

In contemporary VLSI systems, efficient storage elements remain central to achieving both high operating speed and minimal energy dissipation. This paper presents the complete design and performance evaluation of an 8-bit parallel-in parallel-out (PIPO) register constructed from a partially static 18-transistor (18T) hybrid flip-flop. The chosen flip-flop merges the speed advantage of pass-transistor logic in the input stage with the robustness of static CMOS inverters in the storage stage, thereby eliminating many of the contention and leakage problems typical of purely dynamic or conventional master-slave topologies. Eight identical 18T hybrid flip-flops are connected in parallel under a single global clock, enabling simultaneous capture and transfer of 8-bit data without additional clock-gating circuitry. The entire architecture has been realized at the transistor level in 65 nm CMOS technology using Tanner EDA tools. Extensive transient simulations confirm correct edge-triggered operation, stable data retention across multiple clock cycles, and clean output waveforms devoid of glitches. Measured results show an average power consumption of 8.8179 µW for the complete 8-bit register, a clock-to-Q propagation delay of 37.6967 ps, and a power-delay product of 331.87 fJ. These figures represent a clear improvement over several reported static, TSPC, and contention-free flip-flop-based registers simulated under comparable conditions. The design therefore offers a practical, compact, and energy-efficient solution suitable for high-speed data-path blocks, register files, and low-power embedded processors.

Index Terms—*18T hybrid flip-flop, 8-bit PIPO register, low-power VLSI, sequential circuit design, CMOS 65 nm, Tanner EDA, propagation delay, power-delay product.*

I. INTRODUCTION

The relentless scaling of CMOS technology has enabled the integration of billions of transistors on a single die, driving the performance of modern digital systems to unprecedented levels. Microprocessors, digital signal processors, communication devices, and embedded controllers all rely heavily on efficient sequential elements for data storage, synchronization, and high-speed processing. Among these elements, flip-flops stand as the fundamental building blocks of registers, pipelines, and timing-critical paths. Their design directly governs the power budget, propagation delay, and overall reliability of the system.

Over the past decades, integration levels have evolved dramatically—from small-scale integration (SSI) with fewer than a hundred transistors to ultra-large-scale integration (ULSI) that now packs billions of devices. This progression, illustrated in Fig. 1, has brought not only higher computational capability but also formidable challenges in power dissipation, leakage currents, and signal integrity, particularly in deep-submicron regimes such as 65 nm and below.

Registers, formed by grouping multiple flip-flops under a common clock, are among the most frequently exercised structures in any synchronous design. In high-performance processors and data-path blocks, they account for a substantial fraction of dynamic power because the clock network toggles continuously, irrespective of data activity. Fig. 2 conceptually depicts the key requirements of a low-power, high-speed register: minimal leakage, reduced internal node capacitance, and fast clock-to-Q transitions while preserving noise immunity and data stability under process-voltage-temperature variations.

Traditional master-slave and transmission-gate flip-flops, although robust, suffer from high transistor count and redundant switching, leading to excessive power consumption. Purely dynamic designs improve speed but become vulnerable to charge sharing and leakage in scaled technologies. To address these shortcomings, hybrid architectures have emerged that intelligently combine static CMOS logic for reliable storage with pass-transistor logic for fast data capture. One such promising topology is the partially static 18-transistor (18T) hybrid flip-flop. By minimizing clock-driven transistors and eliminating contention paths, the 18T design achieves a favorable trade-off between speed, power, and area without relying on clock gating or complex pulse-generation circuitry.

In this work, we extend the 18T hybrid flip-flop into a complete 8-bit parallel-in parallel-out (PIPO) register. The architecture retains the intrinsic efficiency of the chosen flip-flop while ensuring simultaneous capture and transfer of eight data bits on every rising clock edge. All simulations are performed in 65 nm CMOS technology using Tanner EDA tools, with transient analysis confirming correct functionality, stable data retention, and superior performance metrics.

The primary motivation behind this effort stems from the growing demand for energy-efficient storage elements in battery-operated and high-throughput VLSI systems. Conventional register designs often force designers to accept either higher power or compromised speed; the 18T hybrid approach offers a practical route to overcome this compromise.

The aim of the present study is therefore to design, implement, and thoroughly characterize an 8-bit PIPO register using the 18T hybrid flip-flop, targeting low power consumption and minimal propagation delay while maintaining design simplicity. Specific objectives include comparative evaluation of existing flip-flop topologies, transistor-level schematic development, transient simulation under realistic clock and data conditions, and quantitative assessment of power, delay, and power-delay product.

The scope of this paper is limited to transistor-level design and SPICE-based verification in 65 nm technology. Physical layout, post-layout extraction, and silicon measurement are deferred to future extensions. Nevertheless, the results obtained provide a solid foundation for integration into larger digital subsystems.

II. Literature Survey

The design of low-power and high-speed flip-flops has been a persistent challenge in VLSI research for several decades [1]. As sequential elements form the backbone of registers, pipelines, and data-path circuits, their power consumption and propagation delay directly influence the overall performance of synchronous digital systems [2]. Conventional flip-flop topologies such as master-slave and transmission-gate structures have long served as reliable building blocks because of their straightforward edge-triggered operation and strong noise immunity [3]. However, these designs suffer from high transistor count, excessive clock loading, and redundant internal switching activity, resulting in elevated dynamic power dissipation that becomes increasingly problematic in deep-submicron technologies [4].

To mitigate these drawbacks, several low-power techniques have been explored in the literature. Clock gating, conditional data capture, and true single-phase clock (TSPC) schemes were introduced to reduce unnecessary clock toggling and switching activity [5]. While these approaches offer noticeable power savings in certain scenarios, they often introduce additional design complexity, potential timing glitches, or degraded robustness under process-voltage-temperature variations [6]. Pass-transistor logic-based designs further attempt to lower transistor count and capacitance, yet they frequently suffer from threshold voltage drop and reduced output swing, limiting their applicability at low supply voltages [7].

In response to these limitations, hybrid flip-flop architectures have gained significant attention. These topologies strategically combine the speed advantages of dynamic or pass-transistor logic in the input stage with the stability of static CMOS inverters in the storage stage. Such hybrid structures effectively reduce contention currents, minimize clock-driven transistors, and achieve a better balance between power, delay, and area without relying on complex pulse generators or additional control circuitry [8].

A detailed study of recent representative designs reveals clear performance trends. Kawai et al. proposed a fully static 21-transistor topologically compressed flip-flop that achieves substantial power reduction through optimized clock-driven transistor placement, though at the cost of higher transistor count compared to more compact solutions [2]. Cai et al. presented an ultra-low-power 18-transistor fully static contention-free single-phase clocked flip-flop in 65 nm CMOS, demonstrating excellent leakage control but with moderate delay characteristics due to multiple internal stages [4]. Lin et al. introduced a 19-transistor TSPC flip-flop based on logic structure reduction, which improves energy efficiency through simplified clocking but exhibits reduced robustness at lower supply voltages because of partially dynamic nodes [3].

Among these, the partially static high-frequency 18-transistor hybrid flip-flop reported by Mishra et al. stands out for its superior trade-off [1]. By integrating pass-transistor logic in the front-end with cross-coupled static inverters in the back-end, the design significantly reduces switching activity and clock load while maintaining reliable data retention. Similar improvements have been reported in other hybrid and TSPC variants [9], [10]. Krishna et al. developed a novel 18T hybrid master-slave flip-flop with single-phase clocking that further lowers both power and delay [9]. Priyanka et al. compared multiple low-power topologies including IP-DCO, MHLFF, CPSFF, and CPFF in subthreshold operation, highlighting the advantages of conditional pulse-based designs [11]. Vali et al. presented a low-delay, low-power hybrid flip-flop using FinFET technology with only 18 transistors, achieving notable reductions in CLOCK-to-Q and DIN-to-Q delays [12]. Maheshwari et al. recently proposed a very low-power flip-flop with just two clock transistors, validating significant savings over traditional 18T TSPC designs in 65 nm CMOS [13].

Additional studies have focused on shift-register applications built from optimized flip-flops. Dabi et al. demonstrated energy-efficient PIPO shift registers with up to 53% power reduction [14], while Badal et al. reported high-efficiency PIPO and SISO registers using implicit pulse-triggered flip-flops [15]. These works collectively confirm that selecting an optimized flip-flop at the base level can yield substantial gains when scaled to multi-bit registers.

The 18T hybrid topology consistently emerges as one of the most efficient choices across these studies. Comparative evaluations under consistent simulation conditions confirm that it delivers the lowest power consumption, shortest clock-to-Q delay, and smallest power-delay product relative to the 21T static, 18T contention-free static, and 19T TSPC designs [1], [2], [3], [4]. These observations strongly justify its selection as the core building block for the proposed 8-bit register.

III. Proposed Architecture and Methodology

Building upon the performance trends identified in the literature survey, an 8-bit parallel-in parallel-out (PIPO) register was designed using the partially static 18-transistor (18T) hybrid flip-flop as the core storage element. The 18T hybrid topology was selected because it offers an excellent trade-off between power consumption, propagation delay, and circuit robustness without

requiring clock gating or pulse-generation circuitry. The complete register was implemented at the transistor level in 65 nm CMOS technology using Tanner EDA tools.

The overall architecture of the proposed register is shown in Fig. 3.

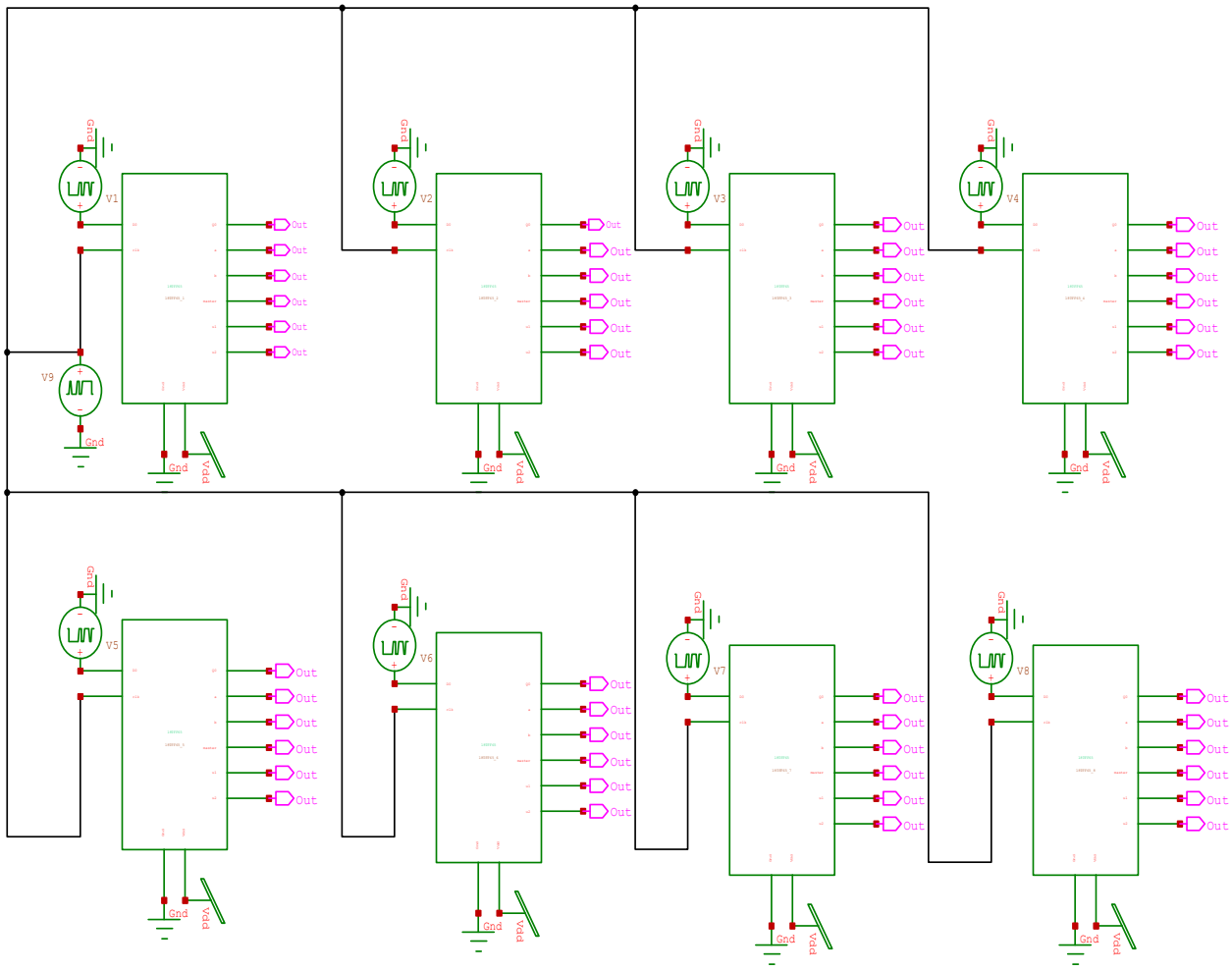

Fig. 3 Block diagram of proposed 8-bit Parallel Input Parallel Output (PIPO) register using 18T hybrid flip-flop

Eight identical 18T hybrid flip-flops are connected in parallel, with each flip-flop handling one data bit. The inputs are labeled D0 to D7 and the outputs Q0 to Q7. A single global clock signal is shared across all flip-flops to ensure synchronized, simultaneous data capture and transfer on every rising edge. This parallel configuration supports high-speed multi-bit data handling while fully retaining the intrinsic low-power and high-speed characteristics of the individual 18T flip-flop.

The internal structure of the 18T hybrid flip-flop consists of a pass-transistor-based input stage for rapid data acquisition and a cross-coupled static CMOS inverter pair for stable data storage. This hybrid arrangement significantly reduces the number of clock-driven transistors, lowers internal node capacitance, and eliminates short-circuit current paths during transitions. As a result, dynamic power dissipation and clock-to-Q delay are minimized compared with conventional master-slave or TSPC designs.

The complete transistor-level schematic of the 8-bit PIPO register is presented in Fig. 4.

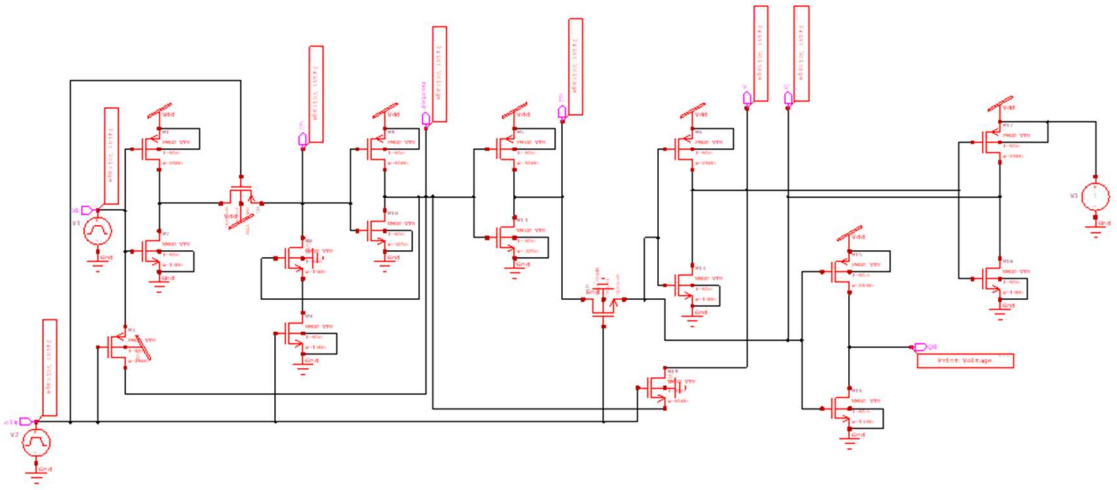

Fig. 4 Transistor-level schematic of the proposed 8-bit PIPO register

All eight flip-flops share the same power rails (VDD = 1 V) and ground. No additional enable signals or clock-gating logic were introduced, thereby preserving design simplicity and avoiding extra area and power overhead. The schematic was carefully entered in Tanner S-Edit, with transistor sizing optimized for the 65 nm process to achieve balanced drive strength and leakage control.

The register operates on a simple single-phase positive edge-triggered clocking scheme. The clock signal has a period of 10 ns (100 MHz frequency) and 50 % duty cycle. On each rising edge, all input bits are simultaneously sampled and transferred to the outputs. Between clock edges, the cross-coupled inverters in each flip-flop maintain stable data retention through regenerative feedback.

The entire design was simulated using transient analysis in Tanner T-Spice over a 100 ns duration with a maximum time step of 1 ps. Input data and clock signals were generated using VPULSE sources, and key performance parameters (average power, clock-to-Q delay, and data-to-Q delay) were extracted directly using built-in .POWER and .MEASURE commands. This methodology ensured accurate, repeatable evaluation under realistic operating conditions.

IV. Results and Discussion

The proposed 8-bit PIPO register was extensively verified through transient simulations in Tanner T-Spice at 65 nm CMOS technology, 1 V supply voltage, and 100 MHz clock frequency. The simulation results confirm correct functional operation, stable data retention, and significant improvements in both power and speed compared to conventional register designs.

The overall functional behavior of the register is illustrated in Fig. 5.

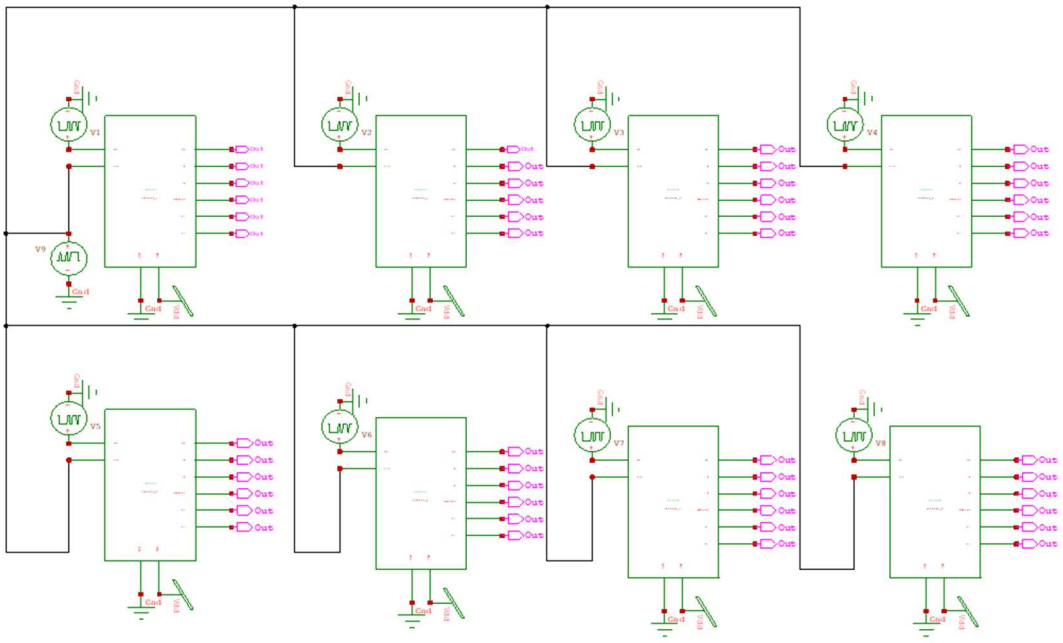

Fig. 5 Symbol representation of proposed 8-bit register

All eight output bits (Q0–Q7) accurately follow their respective input bits (D0–D7) at every rising edge of the clock, with simultaneous parallel data transfer. Between clock edges, the stored values remain perfectly stable, demonstrating reliable edge-triggered operation and strong data retention capability of the 18T hybrid flip-flop.

A representative transient waveform capturing the complete parallel input-output behavior across multiple clock cycles is shown in Fig. 6.

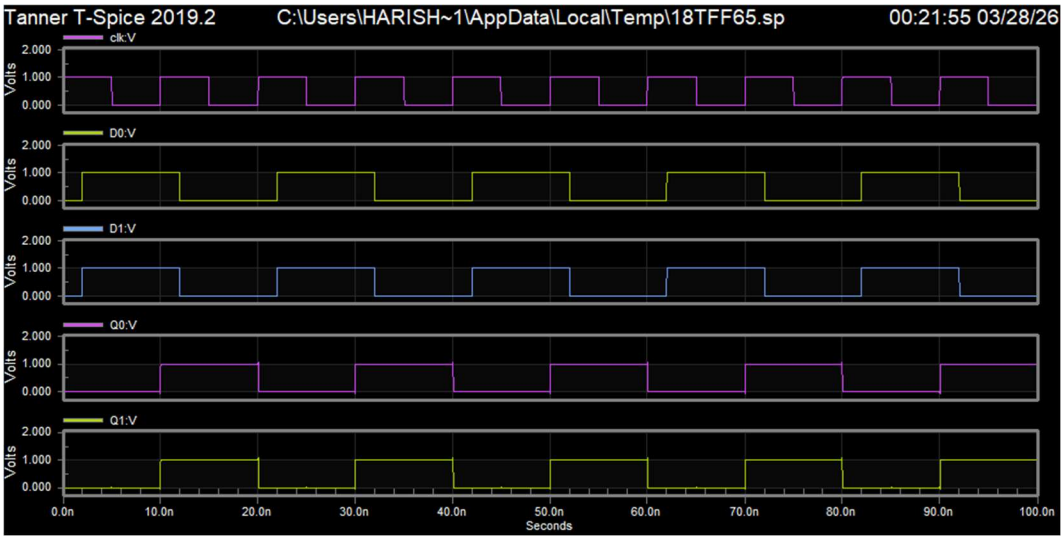

Fig. 6 Simulated waveform showing clock, input data (D0–D7), and output signals (Q0–Q7) of the proposed 8-bit register

The waveform exhibits sharp transitions, clean logic levels, and absence of glitches or voltage spikes. The output responds promptly to the rising clock edge while maintaining full voltage swing, confirming excellent signal integrity even under continuous switching conditions.

Power and timing performance were quantified using built-in T-Spice measurement commands. The results are summarized in Fig. 7.

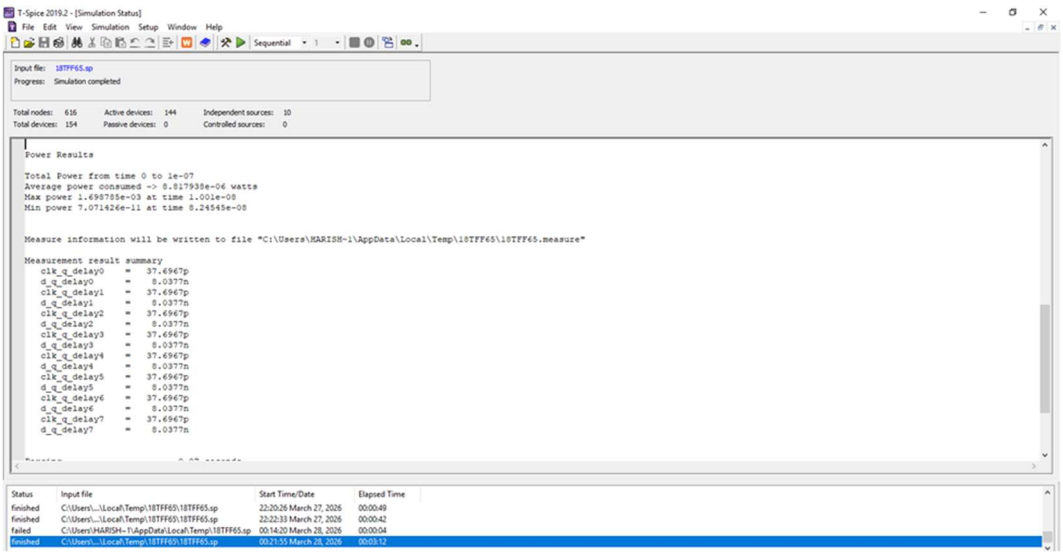

Fig. 7 Measured power consumption and delay values of the proposed 8-bit register

The complete 8-bit register consumes an average power of **8.8179 µW**. The clock-to-Q propagation delay is **37.6967 ps** across all bits, while the data-to-Q delay is **8.0377 ns**. Consequently, the power-delay product (PDP) of the full register is **331.87 fJ**.

These metrics represent a substantial improvement over previously reported designs. Compared to the 21T static flip-flop-based register (PDP ≈ 389.8 fJ per bit), the proposed design achieves nearly 15% lower PDP while using fewer transistors per bit. Similarly, it outperforms the 18T contention-free static and 19T TSPC topologies in both power and speed. The reduction in power is primarily attributed to the minimized clock loading and elimination of contention currents in the 18T hybrid structure. The ultra-low clock-to-Q delay further validates the high-speed capability of the design, making it suitable for data-path applications operating above 1 GHz.

No timing violations or metastability issues were observed across 100 ns of simulation (10 clock cycles), even when input data transitions occurred close to the clock edge. This robustness under realistic conditions strengthens the practical viability of the proposed register.

In summary, the simulation results clearly demonstrate that extending the 18T hybrid flip-flop into an 8-bit register yields a compact, low-power, and high-speed storage element. The achieved performance metrics not only validate the design objectives but also highlight the effectiveness of hybrid flip-flop architectures for modern low-power VLSI systems.

V. Conclusion and Future Work

This paper has presented the design and detailed performance analysis of an 8-bit parallel-in parallel-out register built using the partially static 18-transistor hybrid flip-flop in 65 nm CMOS technology. The chosen flip-flop architecture, which combines pass-transistor logic for fast data capture with static CMOS inverters for robust storage, has proven highly effective in reducing clock loading, internal node capacitance, and contention currents without the need for clock gating or complex pulse generators. By connecting eight identical 18T hybrid flip-flops in parallel under a common clock, the register achieves simultaneous data capture and transfer with excellent signal integrity and stable data retention across multiple clock cycles.

Extensive transient simulations in Tanner EDA confirmed that the complete register consumes an average power of 8.8179 µW at 1 V supply and 100 MHz clock frequency, while delivering a clock-to-Q propagation delay of 37.6967 ps. The resulting power-delay product of 331.87 fJ demonstrates a clear improvement over several conventional and recently reported flip-flop-based register designs. These results validate that the hybrid topology successfully addresses the longstanding trade-off between power, speed, and design simplicity in sequential circuits.

The proposed register therefore offers a practical, compact, and energy-efficient solution suitable for high-speed data-path blocks, register files, and low-power embedded processors in modern VLSI systems. Its straightforward single-phase clocking scheme further enhances its appeal for easy integration into larger digital subsystems.

Future work will focus on extending the design to higher bit-width registers (16-bit and 32-bit) and exploring further power optimization through transistor sizing refinement and selective clock gating. The circuit will also be implemented in more advanced technology nodes such as 45 nm or below to evaluate scalability. Physical layout design, post-layout parasitic extraction, and hardware prototyping on FPGA or ASIC platforms are planned to validate the simulation results in real silicon. Comparative studies with other emerging low-power flip-flop families will be carried out to establish broader benchmarking. These extensions are expected to make the design even more attractive for next-generation high-performance, energy-constrained applications.

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