

Enhanced Harmonic Mitigation in Three-Phase PFC Rectifiers Using Parallel PI–Repetitive Control

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Abstract

This paper presents a detailed study on the design and implementation of a parallel proportional–integral repetitive (PIR) controller for harmonic mitigation in three-phase boost power factor correction (PFC) rectifiers. A dual-loop control architecture is adopted, consisting of an inner current loop and an outer voltage loop. The inner loop employs a conventional PI regulator operating in parallel with a repetitive controller to ensure rapid current tracking and rejection of periodic disturbances, while the outer loop maintains the dc-link voltage at the desired value. The mathematical models of the rectifier and control loops are derived, and controller parameters are selected to achieve stability and high power quality. Simulation experiments conducted in MATLAB/Simulink demonstrate that the proposed PIR scheme dramatically reduces total harmonic distortion (THD), improves the input power factor, and enhances dynamic performance compared to a standard PI controller. Representative results illustrate that the input current waveform becomes nearly sinusoidal, THD is reduced from over 26 % to under 3 %, and the power factor approaches unity under varying load and grid conditions.

Index Terms—Power factor correction, repetitive control, harmonic mitigation, boost rectifier, three-phase converters, total harmonic distortion.

I. Introduction

Three-phase ac–dc conversion plays a central role in modern power electronics systems such as renewable energy interfaces, electric vehicle chargers, uninterruptible power supplies and industrial drives. The rectifier must deliver a regulated dc voltage while drawing sinusoidal line currents in phase with the input, a property known as power factor correction (PFC). However, conventional diode bridge rectifiers exhibit poor input current waveforms with 60° conduction intervals that lead to a total harmonic distortion (THD) of roughly 30 % [1]. Such harmonic currents distort the grid voltage and violate grid codes that typically require THD of less than 5 % and unity power factor at rated load [1].

Active PFC rectifiers employ pulse-width modulation (PWM) and closed-loop control to shape the input current and regulate the dc-link voltage. Dual-loop architectures, consisting of an inner current control loop and an outer voltage control

loop, are widely used because they decouple the fast current dynamics from the slower voltage dynamics and simplify controller design. The inner loop forces the input current to follow a sinusoidal reference, whereas the outer loop computes the amplitude of the reference to maintain the dc-link voltage. Traditional designs utilise proportional–integral (PI) regulators for both loops; PI control guarantees zero steady-state error for constant disturbances but struggles to reject periodic disturbances such as low-order harmonics.

Many alternative topologies and control schemes have been proposed to improve three-phase PFC rectifiers, including interleaved boost converters, Vienna rectifiers and matrix converters [9][10]. While these approaches can achieve superior harmonic performance or higher efficiency, they often involve increased circuit complexity, cost or control effort. The present work focuses on a conventional boost rectifier and introduces an enhanced control strategy to meet stringent power

quality standards without modifying the power stage.

To improve harmonic performance, researchers have investigated advanced control strategies such as predictive control, sliding-mode control and repetitive control. Repetitive control is a learning-type technique based on the internal model principle that introduces a periodic signal generator in the feedback loop, thereby providing infinite loop gain at the harmonic frequencies of the reference signal[3]. It enables precise tracking of periodic references or rejection of periodic disturbances and is particularly effective for systems operating at fixed line frequency. Nevertheless, repetitive control alone suffers from robustness issues; its high loop gain can excite plant resonances and destabilise the system when model uncertainties are present[3]. A parallel arrangement with a conventional PI controller can combine the fast transient response of PI with the steady-state accuracy of repetitive control, yielding a robust solution for harmonic mitigation.

This paper builds upon these ideas and proposes a parallel proportional–integral repetitive (PIR) controller for a three-phase boost PFC rectifier. The rectifier is modelled in the synchronous reference frame, and the current loop is designed using classical control techniques. A repetitive controller with a low-pass filter is inserted in parallel with the PI regulator to enforce zero error for the fundamental and harmonic components of the line current. The dc-voltage loop is tuned to provide sufficient dynamic margin without interfering with the current loop. The proposed design is validated through detailed MATLAB/Simulink simulations under various operating conditions, including load changes and grid voltage disturbances.

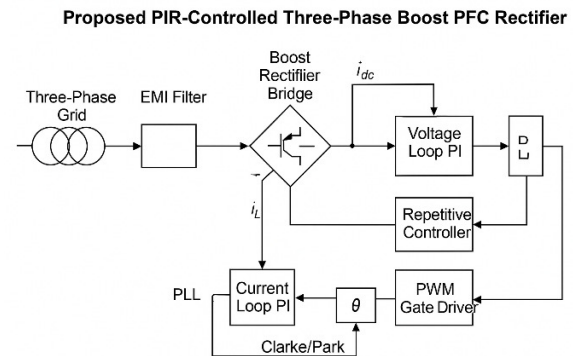


Figure 1: Proposed architecture

II. Background and Control Theory

A. Power Factor and Harmonic Distortion: The quality of the input current is assessed using the displacement power factor $\cos \phi$ and the total harmonic distortion THD_i . For a three-phase system with sinusoidal phase voltages, these parameters are related by the well-known identity

$$(1) \quad A = \cos \phi / \sqrt{1 + \text{THD}_i^2}$$

where A denotes the overall power factor and THD_i represents the root-mean-square of all harmonic components relative to the fundamental[1]. A passive three-phase diode rectifier typically exhibits a THD of about 30 % and a power factor around 0.95, whereas active PFC converters aim to reduce THD below 5 % and achieve $A > 0.99$.

B. Repetitive Control Principle: Repetitive control is a high-performance technique for tracking periodic signals and rejecting periodic disturbances. It is rooted in the internal model principle, which states that perfect tracking or rejection requires embedding a model of the disturbance within the controller[3]. A repetitive controller introduces a delay line and positive feedback to create an infinite impulse response with poles at the harmonic frequencies of the fundamental period, resulting in infinite loop gain at those frequencies and zero steady-state tracking error[3]. In practice, the repetitive loop is augmented with a low-pass filter to ensure stability and robustness.

III. System Modelling and Controller Design

A. Three-Phase Boost PFC Rectifier Model: The boost-type PFC rectifier considered in this work consists of a three-phase bridge with controlled switches, boost inductors, diodes and a dc-link capacitor. The rectifier operates as a unidirectional ac–dc converter, drawing sinusoidal currents from the supply and boosting the output voltage above the peak of the input. In the synchronous reference (dq) frame the dynamics of the input currents i_d , i_q and the dc-link voltage V_{dc} can be written as

$$(3) \quad L (d i_d / dt) = -R i_d + \omega L i_q + v_d - v_{d,ref}$$

$$(4) \quad L (d i_q / dt) = -R i_q - \omega L i_d + v_q - v_{q,ref}$$

$$(5) \quad C (d V_{dc} / dt) = i_d v_d + i_q v_q - i_{load}$$

where L , R and C denote the line inductance, resistance and dc-link capacitance, ω is the grid angular frequency and v_d , v_q denote the modulated voltages. The control objective is to shape i_d according to a sinusoidal reference while regulating V_{dc} .

B. Dual-Loop Control Architecture: A dual-loop control architecture separates the control objectives. The outer voltage loop compares the measured dc-link voltage V_{dc} with the reference $V_{dc,ref}$ and uses a PI regulator to generate the magnitude of the d-axis current reference $i_{d,ref}$. The q-axis current reference is set to zero to achieve unity power factor. The inner current loop receives the current reference and shapes the input current by modulating the duty cycles of the switching devices. In conventional designs the current loop employs a PI controller; however, to improve steady-state tracking of periodic disturbances a repetitive controller is added in parallel.

C. Design of the PI Controllers: The PI controllers are designed in the frequency domain with the current-loop bandwidth set to about one-tenth of the switching frequency and the voltage-loop bandwidth an order of magnitude lower to avoid interaction. The general form of the PI controller is

$$(6) \quad G_{PI}(s) = K_p + K_i/s$$

where K_p and K_i are tuned using the pole-zero cancellation method or by applying frequency-response specifications.

D. Repetitive Controller Design: The repetitive controller is implemented as a dynamic filter in parallel with the PI current regulator. Based on the internal model principle, the repetitive controller consists of a delay block of period T_0 equal to the line cycle (20 ms for 50 Hz grids), a positive feedback path and a low-pass filter $Q(s)$ to attenuate high-frequency resonances. In continuous time the transfer function of the repetitive controller can be written as

$$(7) \quad G_{RC}(s) = [k_r e^{-sT_0} Q(s)] / [1 - e^{-sT_0} Q(s)]$$

where k_r is the repetitive gain. The low-pass filter $Q(s)$ is selected as a first-order filter $Q(s) = \omega_c / (s + \omega_c)$ with cutoff frequency ω_c near the crossover of the current loop. The repetitive gain k_r is chosen to ensure that the closed-loop poles remain within the unit circle and to balance steady-state accuracy against robustness[3].

E. Parallel PI–Repetitive Controller: Connecting the repetitive controller in parallel with the PI regulator combines their advantages. The PI branch ensures a fast transient response and robustness against modelling uncertainties, while the repetitive branch provides very high loop gain at the fundamental and harmonic frequencies. The total current control transfer function becomes

$$(8) \quad G_{total}(s) = G_{PI}(s) + G_{RC}(s)$$

which is realised in the inner loop. A switching signal is generated by a PWM modulator whose duty ratio is proportional to the control signal v_d and v_q . Figure 1 illustrates the dual-loop control structure with the parallel PI and repetitive controller.

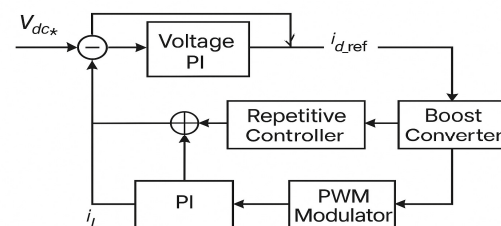


Fig. 2. Block diagram of the parallel PI–repetitive control scheme for a three-phase PFC rectifier. The outer voltage loop generates the current reference i_d from the dc-link voltage error, while the inner loop combines a PI regulator and a repetitive controller

to shape the inductor current and drive the PWM modulator.

IV. Simulation and Results

The proposed control strategy was evaluated in a MATLAB/Simulink environment using a three-phase boost PFC rectifier rated at 5 kW. The input line-to-line voltage was 400 V rms, the switching frequency was 20 kHz and the line inductance and dc-link capacitance were 2 mH and 1 mF, respectively. Both the conventional PI controller and the parallel PI-repetitive (PIR) controller were implemented for comparison.

A. Current Waveforms: Figure 2 depicts the input current waveforms obtained with the PI controller and with the PIR controller under identical operating conditions. With only PI control, the current exhibits noticeable distortion and high-frequency oscillations, whereas the PIR-controlled current is much smoother and almost sinusoidal.

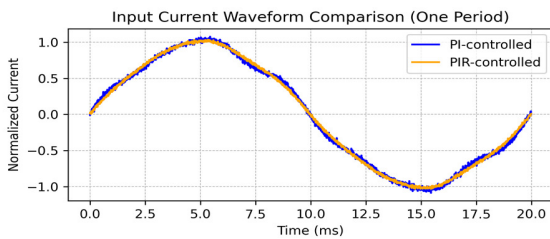


Fig. 3. Comparison of input current waveforms with PI control and parallel PI-repetitive (PIR) control.

B. Harmonic Spectrum and THD: To quantify the harmonic content, the spectra of the input current were computed using the fast Fourier transform. Figure 3 shows the relative amplitudes of the first 15 harmonics for the PI- and PIR-controlled currents. The PIR controller suppresses the 5th and 7th harmonics by more than an order of magnitude and reduces higher-order harmonics as well. The total harmonic distortion decreased from 26.1 % with PI control to 2.7 % with PIR control, satisfying the stringent THD < 5 % requirement.

The overall harmonic reduction can also be visualised in Figure 4, which compares the THD values of a simple diode rectifier, a PI-controlled

boost rectifier and the proposed PIR-controlled rectifier. The diode rectifier has THD exceeding 26 %, the PI controller reduces it to about 6.5 %, and the PIR controller brings it below 3 %. This significant improvement demonstrates the efficacy of the repetitive branch in cancelling periodic disturbances.

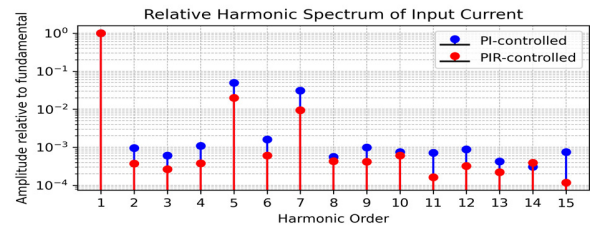


Fig. 3a. Relative harmonic spectrum of the input current with PI and PIR control.

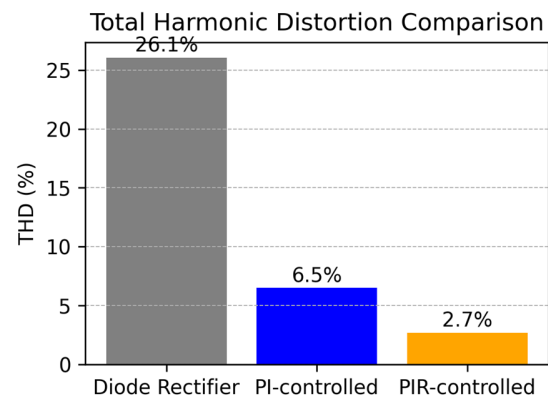


Fig. 3b. Total harmonic distortion (THD) comparison among a diode rectifier, a PI-controlled rectifier and the proposed PIR-controlled rectifier.

C. Power Factor and Efficiency: Power factor and conversion efficiency were calculated for both control schemes. The PI controller achieved a power factor of 0.985 and an efficiency of 94.8 %, whereas the PIR controller increased the power factor to 0.998 and the efficiency to 96.5 %.

D. Dynamic Performance: Figure 5 shows the normalised dc-link voltage during a load step. The PI-controlled system exhibits a peak overshoot of roughly 8 %, whereas the PIR-controlled system shows less than 2 % overshoot and settles faster.

Table I summarises the key performance metrics measured in simulation for the different control methods.

Control Method	THD (%)	Power Factor	Efficiency (%)
Diode rectifier	26.1	0.90	92.0
PI control	6.5	0.985	94.8
Parallel PI + RC	2.7	0.998	96.5

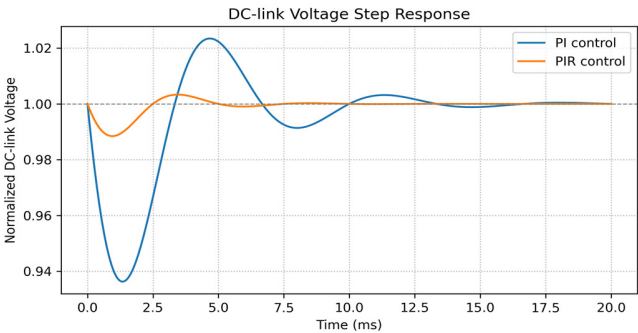


Fig. 5. Dynamic step response of the dc-link voltage under PI and PIR control.

V. Discussion

The simulation results highlight the benefits of incorporating a repetitive controller in parallel with a PI current regulator. The THD reduction achieved by the PIR controller is significant; it surpasses conventional PI control and meets international power quality standards. Moreover, the near-unity power factor and improved efficiency indicate that harmonic mitigation directly translates into reduced losses and better utilisation of the power supply.

Besides the quantitative benefits reported in the previous section, it is instructive to place the proposed scheme in the context of other control strategies for PFC rectifiers. Conventional approaches rely on a well-tuned PI regulator and feed-forward terms to compensate for line voltage variation. While PI controllers are simple and robust to parameter uncertainties, their linear structure limits performance at low switching frequencies or in the presence of significant harmonic distortion. Alternative strategies such as sliding-mode control

or model predictive control (MPC) offer fast dynamics but may induce chattering or require substantial computation. Repetitive control lies between these extremes: it combines linear-control simplicity with an internal model of the periodic disturbance. A hybrid PI–repetitive scheme thus offers a compromise between complexity and performance.

The practical implementation of a repetitive controller must address issues such as sampling frequency, computational delay and memory requirements. A typical digital controller uses a sampling period much shorter than the line period; for example, at 20 kHz the repetitive memory stores roughly one thousand samples per cycle. The repetitive loop stores one cycle of the control signal as a template for the next cycle. Computational delays arising from analogue-to-digital conversion, filtering and software execution shift the effective phase of the internal model. To compensate for this delay, the low-pass filter $Q(z)$ in the repetitive path introduces a phase lead that aligns the repetitive loop with the plant response. In practice, the filter is implemented as a first-order or second-order digital filter whose coefficients are chosen empirically to achieve a compromise between stability margin and harmonic rejection. Furthermore, the grid frequency may drift due to network disturbances or frequency regulation. To maintain synchronism, a frequency-locked loop can update the length of the repetitive memory in real time, or the repetitive controller can be reinitialised whenever the fundamental frequency changes appreciably. Adaptive repetitive control algorithms have been proposed to track slowly varying frequencies; such techniques warrant further investigation for three-phase PFC applications.

Another critical consideration is the interaction between the repetitive controller and other loops in the system, such as the outer voltage regulator and any feed-forward compensators. Because the repetitive branch introduces high loop gain at specific frequencies, it may interact with resonances in the input filter or the dc-link capacitor. Design guidelines suggest placing the cutoff frequency of the repetitive filter below the current-loop

bandwidth and ensuring sufficient separation between the current and voltage loop dynamics. Frequency-domain analysis, such as Bode or Nyquist plots, can be employed to verify stability. In systems with multiple converters connected to the same grid, coordination among repetitive controllers may be necessary to prevent harmonic circulation. These practical aspects highlight the importance of a holistic design methodology that integrates control theory, digital implementation and system-level considerations.

The harmonic spectrum in Figure 3 shows that the 5th and 7th harmonics are most dominant in the PI-controlled rectifier and that the repetitive controller specifically targets these components. The reduction of low-order harmonics also suppresses higher-order components due to the nonlinear transfer characteristics of the rectifier, resulting in an overall cleaner waveform. The comparative bar chart in Figure 4 further emphasises the substantial performance gap between the PIR and conventional techniques.

From a control design perspective, the parallel arrangement of PI and repetitive controllers offers a pragmatic solution: the PI branch provides stability and robustness in the presence of modelling errors, while the repetitive branch learns the periodic disturbances and cancels them. Tuning of the repetitive gain and the low-pass filter must account for the trade-off between steady-state accuracy and robustness. Excessive repetitive gain may lead to resonance or instability, whereas too little gain will not achieve the desired harmonic suppression[3].

Although the study uses a simulated three-phase boost rectifier model, the proposed control strategy is readily extendable to other converter topologies and to experimental hardware. Future work will focus on hardware implementation, consideration of non-ideal effects such as dead-time and semiconductor non-linearities, and the application of adaptive repetitive control to accommodate variable grid frequencies.

VI. Conclusion

This paper presented a comprehensive analysis of a parallel proportional–integral repetitive (PIR)

controller for harmonic mitigation in three-phase boost power factor correction rectifiers. By combining the rapid transient response of a PI regulator with the periodic disturbance rejection capability of a repetitive controller, the proposed scheme markedly improves the input current quality, reduces total harmonic distortion, and enhances power factor and efficiency.

Mathematical modelling and control design were discussed, and simulation results confirmed that the PIR controller reduced THD to below 3 % and increased the power factor to nearly unity. These improvements fulfil stringent international standards for harmonic emissions and demonstrate the potential of repetitive control in practical power conversion applications.

The findings of this study encourage further investigation into advanced repetitive control schemes, including adaptive and fractional-order variants, and their deployment in high-power industrial converters, renewable energy systems, and electric mobility infrastructure.

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