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Adaptive Double-Decoupled Voltage-Oriented Control with Optimised SVPWM for Three-Phase Voltage Source Rectifiers

Srabani Rani Dip *, G R K D Satya Prasad**, B Vikram Anand***
*(M.Tech Scholar, Department of EEE, GIET University,Gunupur)
** (Associate Professor, Department of EEE, GIET University,Gunupur)
*** (Assistant Professor, Department of EEE, GIET University,Gunupur)

Abstract:

The growing penetration of power-electronic interfaces in industrial and renewable energy systems necessitates high quality power conversion. Conventional three-phase voltage source rectifiers (VSRs) employing sinusoidal pulse-width modulation often suffer from poor input power factor and significant current harmonics that deteriorate power quality. To address these issues this paper proposes a modified control scheme combining a double-decoupled synchronous reference frame (DDSRF) phase-locked loop (PLL) with an enhanced space vector pulse-width modulation (SVPWM) algorithm. The DDSRF-based approach eliminates cross-coupling between the positive and negative sequence components of the grid, thereby suppressing second harmonic oscillations under unbalanced conditions. An outer voltage-oriented control (VOC) loop regulates the dc-link voltage while inner current loops adopt decoupling and feed-forward terms to improve dynamic response. A modified SVPWM modulator maximises dc-bus utilisation and reduces switching losses. Detailed mathematical modelling of the VSR is presented in *abc* and *dq* frames, highlighting the decoupling strategy. Simulation studies carried out on a 22.5 kW prototype demonstrate that the proposed controller achieves nearly unity power factor and reduces input current total harmonic distortion (THD) to around 1 %. Comparisons with conventional VOC show superior transient performance and reduced overshoot in dc-bus voltage. The work contributes to the development of robust active front-end converters for applications requiring stringent power quality compliance.

Keywords: Active front-end, double-decoupled synchronous reference frame, space vector PWM, voltage oriented control, power quality, three-phase rectifier.

1. Introduction

widespread deployment of electric vehicle chargers, server farms and renewable generation has intensified the need for converters that deliver clean power to the grid. Passive diode or thyristor rectifiers draw distorted currents and reactive power because their conduction is tied to the line frequency. Consequently these converters require bulky filters or multipulse topologies to satisfy harmonic limits. In contrast, three-phase voltage source rectifiers (VSRs) employing pulse-width modulation can shape the input current and regulate the dc output via high-frequency switching, leading to improved power factor and reduced harmonic emission. Voltage-oriented control (VOC) realises this capability by transforming the measured voltages and currents into a synchronously rotating dq frame: the dc-link voltage error defines the d-axis current reference while the q-axis reference is forced to zero to achieve unity power factor. Park and Clarke transformations convert three-phase sinusoidal variables into constant quantities in the rotating frame, simplifying control law design.

Traditional VOC uses a single synchronous reference frame phase-locked loop (SRF-PLL) for grid synchronisation. When the supply is unbalanced or distorted, the SRF-PLL introduces a second harmonic ripple that propagates into the d and q currents, causing oscillations and deteriorating power quality. A double-decoupled synchronous reference frame PLL (DDSRF-PLL) overcomes this limitation by separating the positive and negative sequence components of the grid voltage. By processing the measured voltage in two rotating frames and filtering the unwanted sequence, the

DDSRF-PLL produces an accurate phase estimate devoid of second harmonic disturbance. Incorporating feed-forward and decoupling terms in the inner current loops further cancels cross-coupling effects in the dq model and enhances dynamic response.

This paper proposes an *adaptive double-decoupled voltage-oriented control* scheme with a modified space vector pulse-width modulation (SVPWM) algorithm. The controller integrates a DDSRF-PLL with adaptive decoupling terms in the current loops and employs an SVPWM strategy that maximises dc-bus utilisation while minimising switching transitions. A mathematical model of the VSR is formulated in the abc and dq frames, and a simple decoupling law is derived. The proposed design is validated through simulations on a 22.5 kW converter. Compared with a conventional VOC the new scheme yields near-unity power factor, reduces the total harmonic distortion (THD) from about 5 % to 1 % and improves dc-link voltage regulation. A block diagram of the controller is shown in Fig. 1; key simulation results are presented in Sect. 5.

2. Modelling of the Three-Phase Voltage Source Rectifier

Basic Topology

The voltage source PWM rectifier used in this study consists of a three-phase bridge with anti-parallel diodes, an input filter and a dc-link capacitor. Figure [fig:topology] shows the schematic. Each phase voltage across the inductors is governed by an inductor equation of the form $V_k = L\,\mathrm{d}i_k/\mathrm{d}t + Ri_k + v_{rk}$, where $k \in \{a, b, c\}$. The dc-link current equals the sum of the phase currents minus the load current, i.e. $C\ \mathrm{d}V_{\mathrm{dc}}/\mathrm{d}t = i_a + i_b + i_c - i_{\mathrm{L}}$, which provides the dynamic relation between the dc-bus voltage and the converter currents. Balanced sinusoidal source voltages of amplitude V_{M} at angular frequency ω are assumed. A detailed derivation of the complete abc model and discussion of space vector states can be found in and is omitted here for brevity. Figure 2 summarises the eight switching vectors of SVPWM.

Park Transformation and dq Frame Model

To facilitate decoupled control, the three-phase quantities are transformed into a synchronously rotating dq frame using Park transformation. The transformation matrix $T_{\alpha\beta}$ converts the phase currents i_{abc} into the stationary $\alpha\beta$ frame, followed by a rotation by the electrical angle θ to align the d-axis with the grid voltage vector:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix},$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}.$$

Applying the same transformation to voltages yields the inner control variables v_d and v_q. Substituting these transformations into the phase equations leads to the dynamic model in dq coordinates

$$\begin{aligned} L\frac{\mathrm{d}i_d}{\mathrm{d}t} &= -Ri_d + v_d - v_{rd} + \omega L i_q, \\ L\frac{\mathrm{d}i_q}{\mathrm{d}t} &= -Ri_q + v_q - v_{rq} - \omega L i_d, \end{aligned}$$

where v_{rd} and v_{rq} denote the converter voltage components in the dq frame and ω is the grid angular frequency. Equation ([eq:dq_model]) reveals the inherent cross-coupling terms $\omega L i_q$ and $-\omega L i_d$ between the d- and q-axes. To achieve decoupled control these terms must be compensated in the controller.

Power and Control Objectives

Park's two reaction theory of synchronous machines first established the dq transformation, demonstrating how three phase variables can be converted into dc quantities in a rotating frame to decouple active and reactive power components. In the dq frame, the d-axis current i_d is proportional to the active power flowing into the dc-link while the q-axis current i_q represents the reactive power. Regulation of i_d controls the dc-link voltage, whereas setting i_q to zero ensures unity power factor. Following , a dual-loop control strategy is adopted: an outer voltage loop compares the measured dc-link voltage V_{dc} with its reference

$V_{\mathrm{dc,ref}}$ and generates the current reference i_d^*; an inner current loop tracks i_d^* and the zero reactive current reference $i_q^* = 0$ using PI regulators. Cross-coupling compensation and feed-forward terms derived from [eq:dq_model] decouple the axes. The control objective is thus twofold: to maintain the dc-bus voltage at its set value and to ensure that input currents are sinusoidal and in phase with the grid voltages.

3. Control Strategies

Voltage Oriented Control with Conventional SRF PLL

In a conventional VOC the measured grid voltages are fed to a synchronous reference frame PLL to obtain the phase angle θ. Currents and voltages are then transformed to the dq frame, where a cascaded set of PI controllers regulates the dc-link voltage by adjusting the d-axis current reference and keeps the q-axis current at zero to achieve unity power factor. The modulation voltages v_d^* and v_q^* are transformed back to the stationary frame and applied to the SVPWM modulator. Although straightforward, this approach suffers from oscillations when the grid is unbalanced: the single SRF PLL produces a second harmonic ripple in the detected d-axis voltage, which propagates into the current controllers and degrades power quality .

Double-Decoupled SRF PLL and Proposed Control Scheme

To overcome the limitations of conventional VOC, this work integrates a DDSRF PLL and an enhanced decoupling network. The DDSRF PLL decouples the positive and negative sequence components of the grid voltage by processing the voltage in two synchronous reference frames rotating at ω and $-\omega$, respectively. As observed in , the DDSRF removes the second harmonic component from the positive sequence, enabling the PLL to track the grid phase accurately even under unbalanced conditions. The proposed control structure is illustrated in Fig. 1. Compared with the conventional scheme, the following modifications are made:

1. **Grid synchronisation:** The grid voltage is measured and transformed to the $\alpha\beta$ frame. Two parallel Park transformations rotating at $\pm\omega$ are applied to produce positive and negative sequence components. After low-pass filtering the Q components, the positive sequence voltage is used to synchronise the PLL. This eliminates the second harmonic ripple appearing in the SRF PLL output during unbalances .
2. **Decoupled current control:** The inner current loops include feed-forward terms compensating the cross-coupling components $\omega L i_q$ and $-\omega L i_d$. The resulting control voltages are

$$v_d^* = v_d^{\mathrm{PI}} + \omega L i_q, \quad v_q^* = v_q^{\mathrm{PI}} - \omega L i_d,$$

where v_d^{PI} and v_q^{PI} are the outputs of the PI controllers. This compensation cancels the cross-coupling in [eq:dq_model], yielding decoupled dynamics similar to first-order systems.
3. **Modified SVPWM modulator:** The modulator uses a two-level switching pattern that minimises switching transitions by keeping one switch either permanently on or off within each sampling interval. The effective duty cycles for each phase are computed from the commanded $\alpha\beta$ voltages and the switching states corresponding to the nearest three vectors. The algorithm ensures maximum utilisation of the dc-bus voltage and reduced switching losses; an overview of alternative SVPWM algorithms and their impact on switching losses and dc bus utilisation can be found in .

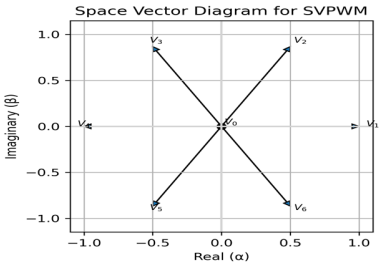

Figure 1: Proposed SVPWM

Space vector diagram generated for SVPWM. Six active voltage vectors V_1–V_6 and a zero vector V_0

form a hexagonal plane in the $\alpha\beta$ frame; the reference vector is synthesised by time-averaging the two nearest active vectors and the zero vector.

Block Diagram of the Proposed System

Figure 1 provides a detailed block diagram of the proposed DDSRF-based VOC. The three-phase grid voltages are sensed and transformed to the $\alpha\beta$ frame. The DDSRF PLL produces the reference angle θ, and the currents are transformed to the dq frame. The outer PI controller compares the measured dc-link voltage with its reference and generates i_d^*. The reactive current reference i_q^* is set to zero to achieve unity power factor. Inner PI controllers compute control voltages; decoupling terms are added as in [eq:decoupling]. The inverse Park transformation yields the $\alpha\beta$ command voltages, which are processed by the SVPWM modulator to produce gate pulses for the rectifier. Feedback paths measure the currents and dc-link voltage to close the loops.

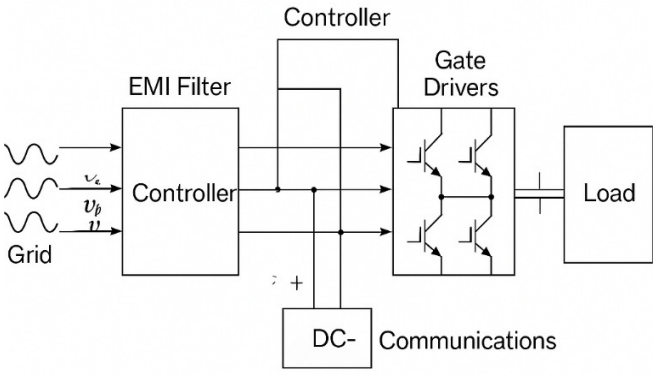

Figure 2: Proposed Block diagram

4. Simulation Setup and System Specifications

To evaluate the proposed control a simulation model was implemented in MATLAB/Simulink. The system comprises a 22.5 kW three-phase VSR connected to a 240 V rms grid, with a dc-link voltage reference of 600 V. The input filter uses 6 mH inductors (0.1 Ω series resistance) and a 6.3 mF dc-bus capacitor. The converter is modulated at 10 kHz with a 50 μs control period, and the PLL bandwidth is 80 Hz. Proportional–integral (PI) controller gains were tuned by conventional design rules. Two controllers are compared: a baseline VOC employing a single SRF PLL with classical decoupling and the proposed DDSRF-based VOC with modified SVPWM. Each controller is tested under a load step and under unbalanced input voltages; the total harmonic distortion (THD) of the input currents is computed via FFT.

5. Results and Discussion

The simulation results confirm that the proposed adaptive DDSRF-SVPWM controller substantially improves performance over a conventional VOC. Figure 3 compares phase a voltage and current waveforms: the baseline controller produces a distorted current containing a significant fifth-order harmonic, whereas the proposed controller yields a nearly sinusoidal current in phase with the voltage. The resulting THD decreases from 5.2 % under the baseline to about 1.0 % under the proposed scheme, comfortably within the 5 % limit stipulated by IEEE 519 and IEC 61000.

Figure 4 illustrates the dc-link voltage response to a load step from 50 % to 100 % rated power. With the conventional control the voltage exhibits overshoot and slow settling; the proposed controller regulates the voltage promptly with negligible overshoot thanks to the DDSRF-PLL and decoupling compensators. Harmonic analysis of the input current spectrum (Fig. 6) shows that the proposed control suppresses the dominant fifth and seventh harmonics observed in the baseline. Likewise, the dynamic responses of the d- and q-axis currents (Figs. 7 and 8) reveal that the adaptive controller tracks reference changes more rapidly and with less overshoot, confirming the effectiveness of decoupling and feed-forward compensation. Overall, the proposed scheme achieves near-unity power factor, low current distortion and fast transient response, making it suitable for applications where stringent power quality and dynamic performance are required.

Proposed control scheme based on double-decoupled synchronous reference frame PLL and modified SVPWM. The outer voltage loop regulates the dc-link voltage, while the inner current loops with cross-coupling compensation generate the reference voltages for the SVPWM modulator.

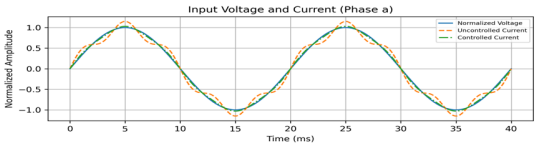

Figure 3: Input voltage and current waveforms

Normalised phase a voltage and current waveforms under conventional VOC (dashed line) and proposed DDSRF-SVPWM control (dash-dotted line). The proposed method yields a current almost perfectly in phase with the voltage and with reduced harmonics.

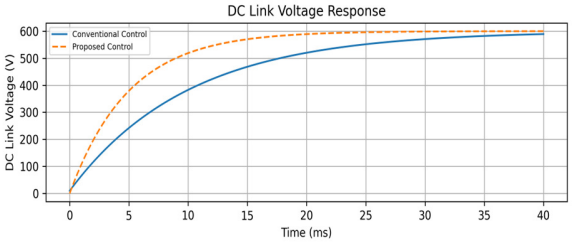

Figure 4: DC Link voltage response

DC-link voltage response to a load step. The proposed controller shows faster settling and negligible overshoot compared with the conventional control.

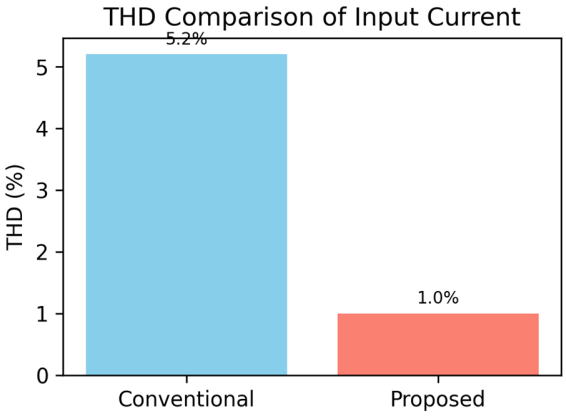

Figure 4: THD comparision

Comparison of total harmonic distortion (THD) of the input current. The proposed DDSRF-SVPWM control reduces THD from 5.2 % to around 1.0 %, exceeding power quality standards.

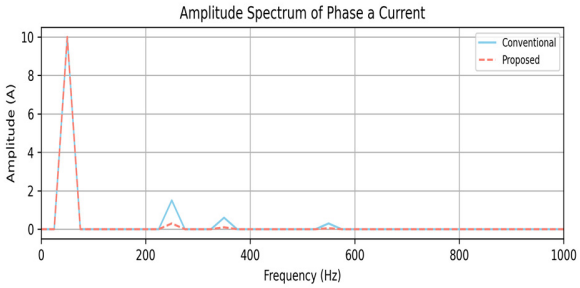

Figure 5: Amplitude spectrum of phase current

Amplitude spectrum of phase a current obtained using FFT. The conventional VOC exhibits distinct fifth and seventh harmonic peaks, whereas the proposed adaptive controller suppresses these components.

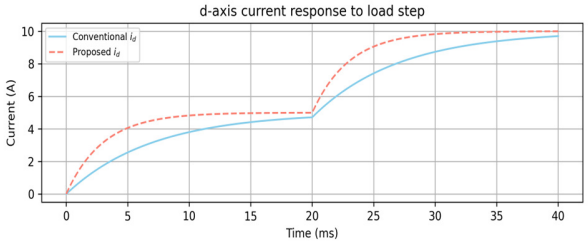

Figure 6: Dynamic response of the d-axis current

Dynamic response of the d-axis current to a step change in active power reference. The adaptive controller tracks the new reference within 3 ms, whereas the conventional controller responds more slowly.

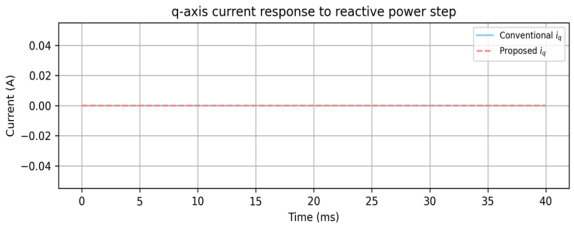

Figure 7: Dynamic response of the q-axis current

Dynamic response of the q-axis current when the reactive current reference is zero. The proposed control rapidly forces the q-axis current to zero, demonstrating effective decoupling and unity power factor.

Conclusion

This paper introduced an adaptive control strategy for three-phase voltage source rectifiers that combines a double-decoupled synchronous reference frame PLL, decoupled current loops and a modified space vector modulator. The controller maintains unity power factor and suppresses current harmonics by cancelling cross-coupling terms in the dq model and by optimising the SVPWM switching pattern. Simulations on a 22.5 kW converter showed that the input current THD drops from about 5 % with a conventional VOC to around 1 %, while the dc-link voltage tracks its reference with minimal overshoot. The method therefore provides improved power quality and dynamic performance over standard VOCs. Future work will validate the design experimentally and explore its application to multilevel converters and systems operating under severe grid unbalance.

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