International Journal of Scientific Research and Engineering Development-– Volume 7 Issue 6, Nov-Dec 2024
Available at www.ijsred.com

RESEARCH ARTICLE OPEN ACCESS

A Sinusoidal Pulse Width Modulation (SPWM) Technique for Capacitor Voltage Balancing of Nested T-Type Four-Level Inverter

Dr. S. Nithya Lavanya,
Senior Lecturer in EEE, Govt. Polytechnic, Anantapur.

----------**********----------

Abstract:

This paper introduces a novel control method based on the sinusoidal pulse width modulation (SPWM) scheme to regulate the capacitor voltages of a four-level T-type NNPC inverter. The four-level T-type NNPC inverter features a reduced number of switches and components compared to other traditional and advanced four-level inverters, making it a compelling choice for high-power, medium-voltage applications. This topology has been analyzed under the assumption of constant DC sources rather than flying capacitors. A simple single-phase modulator is developed to balance the voltages of the flying capacitors. The performance and feasibility of the proposed control technique are experimentally evaluated under steady-state and transient conditions, as well as for various modulation indices and loads. Experimental results confirm the effectiveness of the control method in regulating the capacitor voltages.

----------**********----------

I. INTRODUCTION

Multilevel inverters are very attractive and commonly used for high-power medium-voltage applications [1]-[2]. Neutral- Point clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB) converters are established classical multilevel converter topologies. However, these topologies have inherent limitations that restrict their applications.

- **NPC Topologies:** Managing voltage balance across the DC-link capacitors becomes increasingly challenging as the number of levels grows. Additionally, the number of clamping diodes rises significantly with higher levels.
- **FC Topologies:** Maintaining balanced capacitor voltages requires higher switching frequencies, and the number of capacitors increases with additional levels, reducing the converter's reliability and lifespan.
- **CHB Topologies:** With a modular structure, CHB can achieve higher voltages and more levels by increasing the number of cells. However, it requires multiple isolated DC sources, typically provided by a bulky and costly phase-shifting transformer, and the number of switches grows significantly with higher output levels.

To address these challenges, advanced multilevel topologies have been developed, many of which combine classic designs to mitigate their disadvantages. Examples include the five-level H-bridge NPC (5L-HNPC), three-level active NPC (3L-ANPC), and five-level active NPC (5L-ANPC):

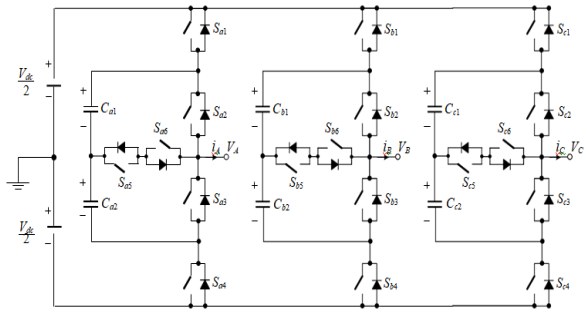
- **5L-HNPC:** Combines two classic 3-level NPCs to form a 5-level converter capable of operating at higher voltage levels than conventional NPCs. However, it requires multiple isolated DC sources and a phase-shifting transformer, adding bulk and cost.
- **3L-ANPC:** Replaces clamping diodes with clamping switches, providing a controllable path for neutral current and balanced loss distribution among switches. While it improves performance, it increases the number of active switches, raising production costs and reducing reliability.
- **5L-ANPC:** A hybrid of 3L-ANPC and 3L-FC, this topology produces more levels and enhances output voltage quality. However, the switches have varying

voltage ratings, complicating design and implementation.

A four-level nested neutral point clamped (4L-NNPC) converter, introduced in recent studies, has fewer components than existing topologies, enhancing its appeal. Recently, the four-level T-type NNPC, shown in Fig. 1, was proposed. This topology stands out for high-power, medium-voltage applications due to its reduced number of components compared to other four-level designs, as summarized in Table I.

TABLE I: COMPARISON NUMBER OF DEVICES AMONG DIFFERENT TOPOLOGIES

Topology	Number of switches	Number of clamping diodes	Number of flying capacitors
NPC	18	18	-
FC	18	-	9
NNPC	18	6	6
T-Type NNPC	**18**	**-**	**6**



As shown in Table I, the T-type NNPC inverter features a reduced number of components, leading to improvements in size, weight, cost, and reliability compared to existing four-level topologies. Previous studies on this inverter, such as [17], analyzed its operation assuming constant DC sources instead of flying capacitors—a scenario that is not practical. In real-world applications, flying capacitors replace DC sources, necessitating a more advanced control method to regulate their voltages.

This letter presents a novel control method based on sinusoidal pulse width modulation (SPWM) to manage and balance the flying capacitor voltages at the desired levels, ensuring the proper operation of the T-type NNPC inverter under various conditions. The effectiveness of the proposed control strategy is analyzed in the MATLAB/Simulink environment and validated experimentally under steady-state and transient conditions across different modulation indices.

The structure of the letter is as follows:

- **Section II:** A brief explanation of the T-type NNPC inverter operation, followed by the application of SPWM for flying capacitor voltage control.
- **Section III:** Development of the proposed control technique.
- **Section IV:** Experimental verification of the feasibility and performance of the proposed controller.

II. OPERATION OF THE NESTED T-TYPE NEUTRAL POINT CLAMPED INVERTER

A four-level T-type NNPC topology combines the flying capacitor topology with a T-type inverter configuration [17]. In this topology, the capacitors Cx1C_{x1} and Cx2C_{x2} (x=a,b,cx = a, b, c) are charged to one-third of the total DC-link voltage. The inverter can produce four output voltage levels through six switching states, as detailed in Table II. Bidirectional switches provide a controllable current path to manage the direction of the output current.

As shown in Table II, levels 2 and 3 have two redundant switching states that generate medium voltage levels of ±1/6Vdc\pm 1/6 V_{dc} with respect to the midpoint of the DC source. Each redundant switching state has a distinct charging or discharging effect on the flying capacitors. Capacitor voltage control is achieved by selecting the optimal redundant switching state, ensuring the capacitors charge or discharge to maintain the

desired voltage of one-third of the total DC-link voltage.

III. Sinusoidal Pulse Width Modulation for a T-Type NNPC Converter

Balancing the capacitor voltages in a T-type NNPC converter is critical to ensuring proper operation under varying conditions. Without control, the flying capacitors may overcharge or discharge during operation, causing their voltages to deviate from the target value and preventing the converter from generating a four-level output voltage.

This section introduces a new control technique based on a sinusoidal pulse width modulation (SPWM) scheme to address this challenge. The deviation of capacitor voltages from the desired value (Vdc/3V_{dc}/3) is expressed as follows:

$$\Delta V_{Cxi} = V_{Cxi} - V_{dc}/3$$

$$x = a, b, c \quad i = 1, 2$$

To maintain balanced capacitor voltages, ΔVCxi\Delta V_{C_{xi}} (x=a,b,c;i=1,2x = a, b, c; i = 1, 2) must be kept at or near zero under all operating conditions. When the voltage deviation is positive, a switching state that discharges the capacitor should be selected. Conversely, if the deviation is negative, a switching state that charges the capacitor should be chosen.

Table II: Switching States of the T-Type Four-Level Inverter and the Impact of AC-Side Currents on Flying Capacitor Voltages.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	V_{Cx1}	V_{Cx2}	V_{xn}	Output Level	State
1	1	0	0	1	0	No Impact	No Impact	$\frac{V_{dc}}{2}$	3	3
1	0	0	0	1	1	Charging (ix>0) Discharging (ix < 0)	No Impact	$\frac{V_{dc}}{6}$	2	2B
0	1	0	1	1	0	Discharging (ix > 0) Charging (ix < 0)	Discharging (ix > 0) Charging (ix< 0)			2A
1	0	1	0	0	1	Charging (ix >0) Discharging (ix < 0)	Charging (ix > 0) Discharging (ix < 0)	$-\frac{V_{dc}}{6}$	1	1B
0	0	0	1	1	1	No Impact	Discharging (ix > 0) Charging (ix< 0)			1A
0	0	1	1	0	1	No Impact	No Impact	$-\frac{V_{dc}}{2}$	0	0

TABLE III: THE PROPOSED VOLTAGE CONTROL METHOD

Output Level	i_x	ΔV_{Cx1}	ΔV_{Cx2}	Condition	State
1	≥ 0	≥ 0	≥ 0	-	1A
			< 0	-	1B
		< 0	≥ 0	$\|\Delta V_{Cx1}\| < \|\Delta V_{Cx2}\|$	1A
				$\|\Delta V_{Cx1}\| > \|\Delta V_{Cx2}\|$	1B
			< 0	-	1B
	< 0	≥ 0	≥ 0	-	1B
			< 0	$\|\Delta V_{Cx1}\| < \|\Delta V_{Cx2}\|$	1A
				$\|\Delta V_{Cx1}\| > \|\Delta V_{Cx2}\|$	1B
		< 0	≥ 0	-	1B
			< 0	-	1A
2	≥ 0	≥ 0	≥ 0	-	2A
			< 0	-	2A
		< 0	≥ 0	$\|\Delta V_{Cx1}\| < \|\Delta V_{Cx2}\|$	2A
				$\|\Delta V_{Cx1}\| > \|\Delta V_{Cx2}\|$	2B
			< 0	-	2B
	< 0	≥ 0	≥ 0	-	2B
			< 0	$\|\Delta V_{Cx1}\| < \|\Delta V_{Cx2}\|$	2A
				$\|\Delta V_{Cx1}\| > \|\Delta V_{Cx2}\|$	2B
		< 0	≥ 0	-	2A
			< 0	-	2A

As shown in Table II, certain switching states result in the capacitors of a phase being charged or discharged simultaneously, posing a challenge for effective voltage control. For instance, at voltage level 1, if the deviation for C1C_1 is positive and the deviation for C2C_2 is negative, and the output current is positive, selecting switching state 1A will charge C2C_2 toward its desired value. However, it will also overcharge C1C_1, further increasing its deviation, which is undesirable.

To address this issue, Table III has been developed to guide the selection of the optimal switching state to maintain capacitor voltages at their target levels. At voltage levels 0 and 3, there are no redundant switching states, and these levels have no impact on capacitor voltages. However, for levels 1 and 2, redundant switching states exist. Based on the current direction and the voltage deviation of the capacitors, the most suitable switching state is chosen using Table III.

For example, when the output voltage level is 1 and i≥0i \geq 0, ΔVC1≤0\Delta V_{C_1} \leq 0, and ΔVC2≤0\Delta V_{C_2} \leq 0, both capacitors need to be charged, so switching state 1B should be selected. The flowchart in Fig. 2 outlines the procedure for controlling the flying capacitor voltages in each phase:

1. Determine the desired output voltage level by comparing the modulation signal with the three carriers used for the four-level converter.

2. Measure the direction of the phase currents and the capacitor voltages.
3. Based on the output voltage level, current direction, and capacitor voltage deviations, select the appropriate switching state from Table III.
4. Finally, generate the gate signals and apply them to the switching devices.

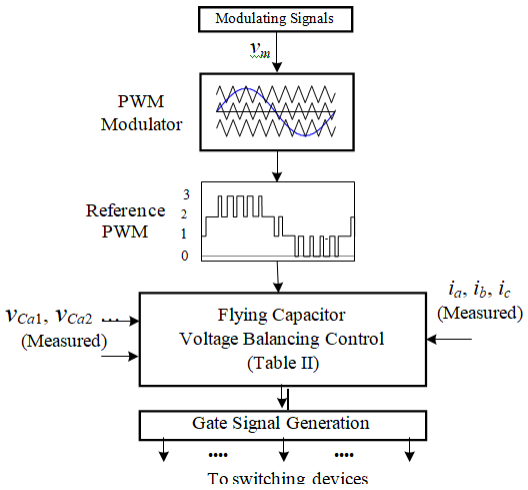


Fig. 2. Block diagram of capacitor voltage balancing control

IV. EXPERIMENTAL RESULTS

The feasibility of the proposed SPWM-based control technique is validated experimentally using a scaled-down prototype, with parameters listed in Table IV.

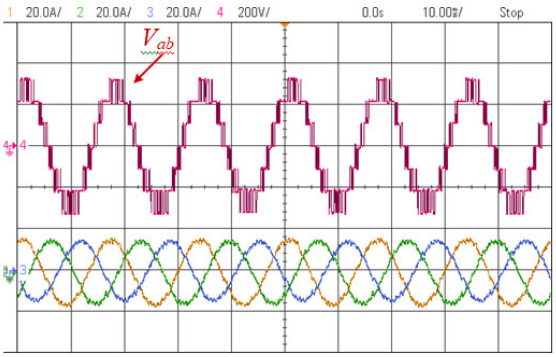
Figures 3 through 6 illustrate the performance of the control technique under both steady-state and transient conditions:

- **Figure 3:** Depicts the inverter's output voltage, output currents, and flying capacitor voltages with a modulation index m=0.9m = 0.9 and load power factor (PF) of 0.9. The total harmonic distortion (THD) of the inverter output voltage is 24.7%.
- **Figure 4:** Shows similar waveforms for m=0.55m = 0.55 and load PF = 0.9, with an inverter output voltage THD of 40.7%.
- **Figure 5:** Demonstrates the converter's performance during a modulation index change from m=0.55m = 0.55 to m=0.9m = 0.9.
- **Figure 6:** Highlights the controller's effect when activated and deactivated. Without the controller, the capacitor voltages deviate significantly, but upon activation, the voltages converge to the desired levels.

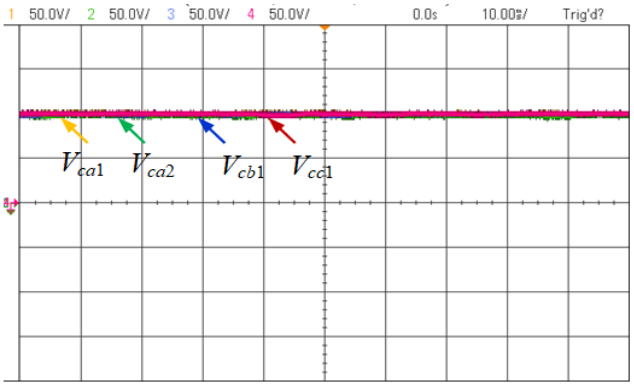
These results, as shown in Figures 3 to 6, confirm the effectiveness of the proposed control technique, demonstrating that all capacitor voltages remain well-balanced under various operating conditions.

TABLE IV: PARAMETERS OF THE STUDY SYSTEM

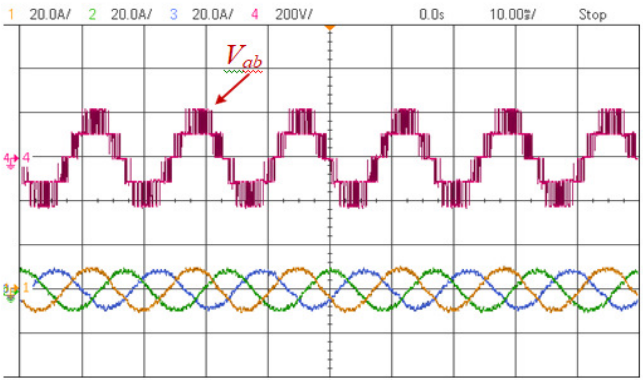
Converter parameters	Values
Converter rating (kVA)	5
Capacitor Value (μF)	2200
Input dc voltage (V)	320
Output frequency (Hz)	60
Output inductance (mH)	5
Output load (Ω)	12



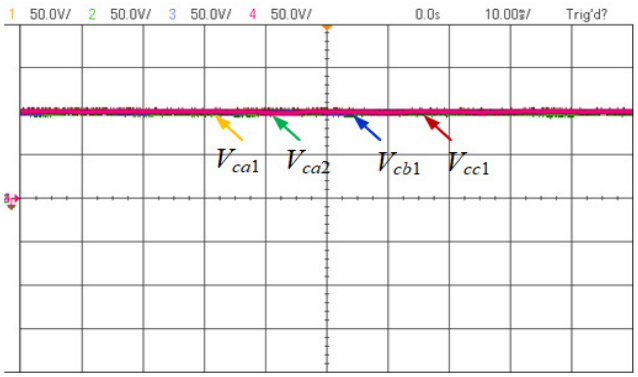
(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)



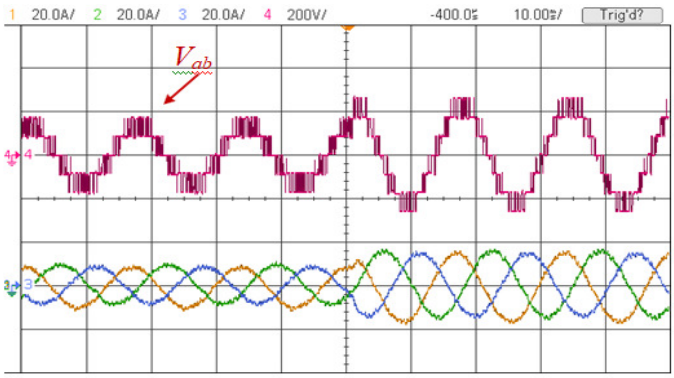
(b) voltages of flying capacitors (50V/div, 10ms/div) Fig. 3. Experimental results, m = 0.9 and PF=0.9.



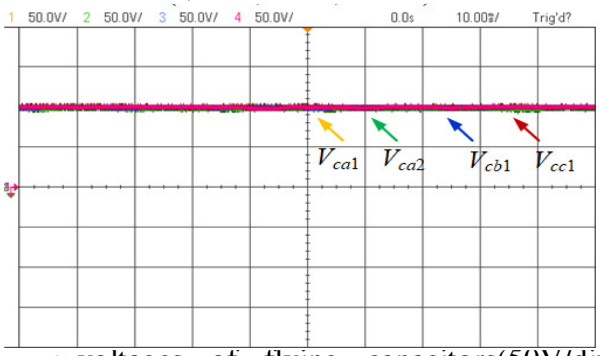
(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)



(b) voltages of flying capacitors (50V/div, 10ms/div) Fig. 4. Experimental results, m = 0.55 and PF=0.9



(a) inverter output line voltage and output currents (200V/div, 10A/div, 10ms/div)



(b) voltages of flying capacitors(50V/div, 10ms/div)

(c) Fig. 5. Experimental results, modulation change from m=0.9 to m=0.55.

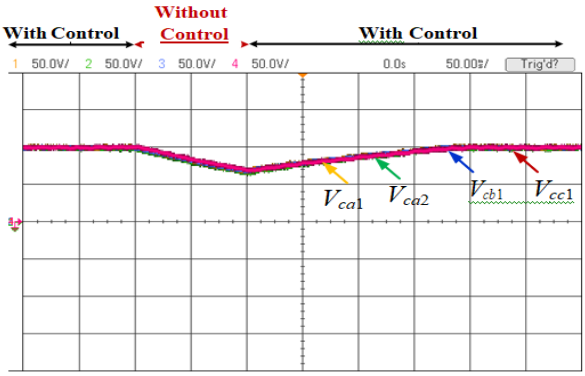


Fig. 6. Voltage of flying capacitor when the controller is deactivated and activated

IV. CONCLUSION

This paper proposes a sinusoidal pulse width modulation (SPWM)-based control method for a topology that is particularly appealing for medium-voltage applications due to its reduced number of components compared to existing designs. The control method

optimally selects the most suitable switching state among redundant states to effectively charge or discharge the flying capacitors, minimizing voltage deviations from their desired levels.

The simplicity of the SPWM-based controller makes it easy to implement. The feasibility of the proposed technique is validated through simulation studies and experimental testing, with the results confirming its effectiveness.

REFERENCES

[1] B. Wu and Mehdi Narimani, High-Power Converters and AC Drives. IEEE Wiley Press, 2017.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553– 2580, Aug. 2010.

[3] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S.Kouro, "Multilevel voltage source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[4] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," *IEEE Trans. on Power Electron.*, vol. 27, no. 2, pp. 652–660, 2012.

[5] Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

[6] J. Shen, S. Schröder, J. Gao and B. Qu, "Impact of DC-Link voltage ripples on the machine-side performance in NPC H- bridge topology, " *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3212-3223, July-Aug. 2016.

[7] V. Michal, "Three-Level PWM Floating H-Bridge Sine wave Power Inverter for High-Voltage and High-Efficiency Applications, " *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4065-4074, June 2016.

[8] T. Bruckner, S. Bernet, and H. Guldner, "The Active NPC Converter and its Loss-Balancing Control, " *IEEE Trans. Industrial Electronics*, Vol. 52, No. 3, pp. 855-868, 2005.

