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RESEARCH ARTICLE OPEN ACCESS

A 31-SEGMENT ASYMMETRICAL CASCADED MULTILEVEL INVERTER

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Abstract:

The 31-level Asymmetrical Cascaded Multilevel Inverter used in this project provides commentary. A single stage sub multilevel converter unit and a complete bridge cascaded multilevel inverter connected in a cascaded manner form the foundation of the topology. Plans are in place for the input DC voltage sources of Vdc1–Vdc4 to be paired at 15 Vdc1, 30 Vdc2, 60 Vdc3, and 120 Vdc4 each. The power semiconductor switches in the asymmetric cascaded multilevel inverter are controlled by a low frequency pulse width modulation method. A DC source feeds the DC link with a higher voltage. With a unidirectional power flow and a high frequency transformer processing up to 33% of the load power, the primary DC link supplies the other, lower voltage dc links. A detailed presentation is made of the HFL system architecture, a nearest-level control, and an analysis of the power distribution among each dc connection. Furthermore, employing HFL, comparisons with alternative multilevel topologies are performed. The system analyses and uses the total harmonic in real time.

Keywords —: Asymmetrical cascaded multilevel inverter, DC source, HFL system, Higher voltage.

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I. INTRODUCTION

A recent development in power converter technology is the multilevel inverter, which finds widespread application in high- to medium-power applications such the integration of renewable energy resources, FACTS devices, and other related fields. A virtually sinusoidal output voltage waveform is obtained. Because multilevel inverters can effectively handle the increased demands for power rating and power quality associated with lower electromagnetic interference and harmonic distortion, they are becoming more and more popular in power electronic applications.

The multilevel inverter may function at both high and fundamental switching frequencies. Multilevel inverters are essentially used in three different topologies: cascaded H-bridge MLI (CHB), flying capacitor MLI (FC), and neutral point clamp MLI (NPC).Despite the need for distinct DC sources for each module, the cascaded H-bridge topology has attracted a lot of interest when compared to alternative topologies such as NPC and FC due to its simplicity and adaptability.

CHB topologies are classified as either symmetric or asymmetric depending on the size of the DC voltages. In comparison to symmetric topology, asymmetric topology uses fewer switches, DC sources, and diodes to achieve the same voltage levels. Given that there are fewer switching devices and less overall harmonic distortion, the suggested MLI design is superior to the current topologies.

The design of an asymmetric multilevel inverter is to maintain a ratio of 1:2:4:8 despite the different DC source magnitudes. Phase disposition pulse width modulation (PD-PWM) is developed using a 2 kHz multiple carrier signal. In this study, a level-shifted PWM scheme that uses independent DC sources and fewer switches is devised. The main way to get a high number of voltage levels with fewer components is to use asymmetric cascade inverters.

They demonstrate that, in comparison to their symmetrical counterpart, they can produce the same number of levels with fewer switches and DC sources. However, limits the applicability in high-voltage scenarios due to the usage of a wide range of ratings for its semiconductor devices and dc links, which results in decreased flexibility.

The primary contributions of this article are twofold: firstly, it presents a method for supplying the cascaded structure with a single dc source using an HFL that is intended to supply the necessary power flow for balancing dc links; secondly, it evaluates the power processed by the HFL by studying the active power distribution among the dc links under various modulation index circumstances. The design of the HFL semiconductor devices and high frequency transformer (HFT), new experimental findings to support the theoretical considerations, and a modulation strategy to enable operation at low modulation indexes when a fixed dc source is used are some of the additional aspects covered in this article.

II. EXISTING SYSTEM

The diagram shows how each sub-multilevel inverter is connected to the others in order to get the desired output voltage and level count. Both IGBT switches and DC voltage sources make up the sub-multilevel inverter. Bidirectional switches and unidirectional switches make up the IGBT switch architecture. Utilizing an anti-parallel diode, the unidirectional switches regulate the Insulated Gate Transistor (IGBT).

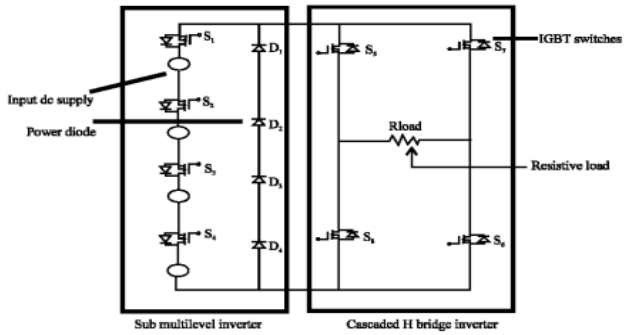

Fig 1: The 31-level asymmetrical multilevel inverter.

At zero voltage, the output is the result of turning on switches S0 and Sc1. V dc is created at the output when the switches S1, Sb1, and Sc1 are turned on. This parallels the two dc voltage sources. In the same way, two DC voltage sources could be linked in series when switches S1 and Sa1 turnon, producing 2Vdc at the output.

Switching states					
Sa1	Sb1	Sc1	S1	S0	Vo
0	0	1	0	1	0
0	1	1	1	0	V dc
1	0	0	1	0	2V dc

Table 1: Switching sequence for basic unit.

III.PROPOSED SYSTEM

It displays the multilevel inverter's suggested topology for the n-level. Three bridges make up this arrangement: a lower H-Bridge with a cascading series/parallel circuit and two top H-Bridges. It illustrates the lower H Bridge's series/parallel circuit working principle. This principle is used to produce an output with a large number of steps. The inverter needs 15 switching devices for each of the 31 levels if the voltage ratio for the 31-level cascaded multilevel inverter voltage sources is 1:2:6. Equation and switching sequence are used to produce the two voltage sources needed for series/parallel circuit levels.

Vout = V1+V2+V3

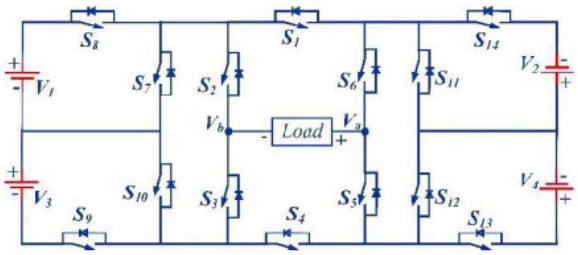

Figure 2: proposed equivalent circuit of 31-level MLI.

The MATLAB/Simulink model of the proposed inverter with 31-level output is shown below. It is clear that distortion goes down as level counts rise. The recommended architecture requires less switches than 19 different topologies.

The suggested architecture is demonstrated to require fewer switches overall. Hence, for a large

number of levels, complexity is decreased. Asymmetric multilevel inverters have the same architecture as their symmetric counterparts. The only things that separate them are the input dc voltage ratings and control strategies. Numerous applications provide challenges when utilizing separate DC sources, and an excessive number of DC sources can lead to lengthy cables and potential voltage imbalance.

. Asymmetrical design, which employs fewer bridges, is suggested as a way to lower the number of dc sources needed for the cascaded H-bridge multilevel inverter.

Since battery cells are the power source in electric vehicles (EVs), the cascaded multilevel inverter, which uses multiple voltage sources, is appropriate. It's possible that the battery cells aren't constantly equal and that their discharge isn't uniform depending on the output requirement. The series fundamental units of the previously suggested topology are made up of connections between dc voltage sources in series and parallel. The dc voltage sources' values vary from one unit to the next.

The suggested asymmetric design of the 31-level MLI topology is tested experimentally in a laboratory by assembling a prototype inverter setup employing four unequal DC supplies with voltage magnitude, R-load, L-load, and switching pulse, in addition to fourteen IGBTs that are triggered.

The magnetic flux density's greatest value is denoted by B_max, whereas A represents the core area. As a result, the principal winding's number of turns can be found using,

$$N\_1 = E/(4.f.A.Bmax)$$

When compared to other options, such as low-frequency transformers, the HFL solution is highly appealing because of its high frequency functioning and the transformer's size, weight, and cost.

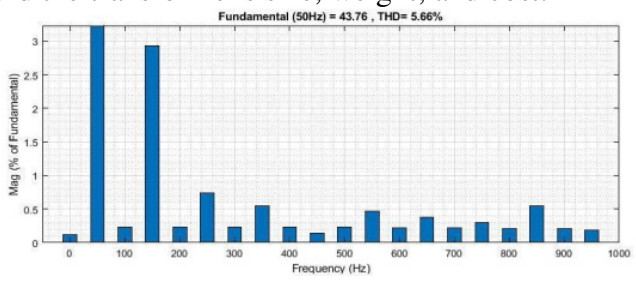

Figure 3: Voltage output for R-load.

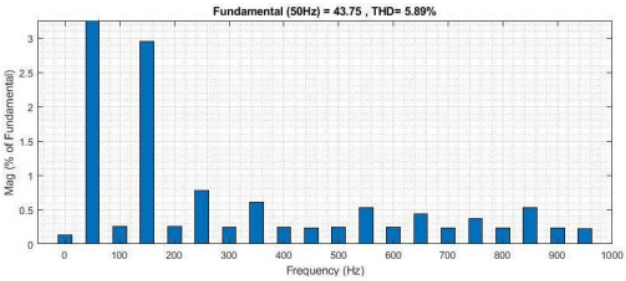

Figure 4: Voltage output for RL-load.

Figures 3 and 4, respectively, demonstrate the results obtained for the R and RL load. To see the consequences of changing the loading, the THD analysis for both loads is observed and examined. The results are displayed.

IV RESULT

The multilayer inverter with asymmetric cascaded switching combination. This circuit uses low frequency pulse width modulation to regulate the 31-level asymmetrical inverter's switches. The absolute sine wave is contrasted with the DC offset. Depending on the type of logical circuit—AND, OR, or NOT. To create the gate pulse, one uses the switching approach. The output levels of this system are one zero, fifteen negative, and fifteen positive switches. This means that the switching pulse from switches S1 through S8 is produced by generating 15 DC offsets and comparing them with an absolute sine wave.

The output voltage level of the 31-level asymmetrical inverter is displayed in the next step. There are two output voltage levels: 15Vdc and -15Vdc. An asymmetric 31-level inverter's switching gate pulse. Low frequency pulse width modulation with DC offset is used in the design of this switching sequence. This switching approach uses low frequency pulse width modulation to lower the switching losses in the system. For a 31-level inverter, the overall harmonic distortion is 3.25%.

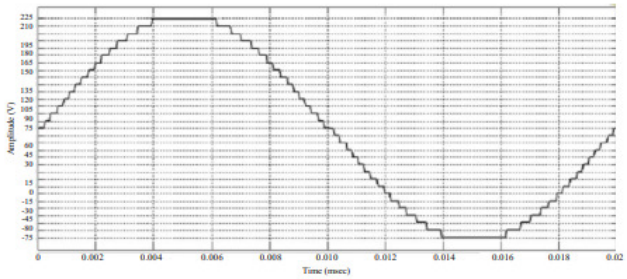

Figure 4: Output voltage of 31-level asymmetrical MLI.

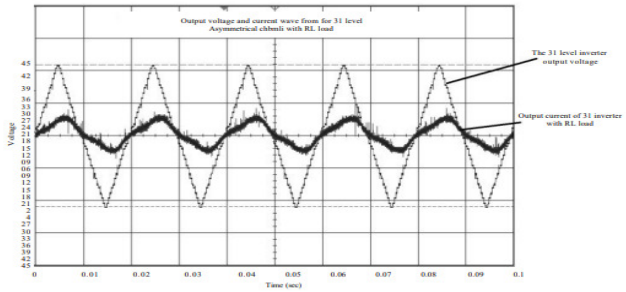

Figure 5: Output voltage and current waveform of 31-level MLI using RL load.

When compared to other harmonics, the first order harmonics in this are extremely high. An analysis of the 31-level inverter's total harmonic distortion using an RL load reveals that it is 18.22%. When compared to other harmonics in this system, the first and third order harmonics are extremely high. The THD research indicates that a 31-level inverter improves system performance.

V. CONCLUTION

This study examines the system's 31-level asymmetrical cascaded H-bridge multilevel inverter. The gate pulse for the inverter is produced by low frequency pulse width modulation techniques. THD analysis for the 15-level inverter is 18.22% for the three DC voltage sources—Vdc1=3 V, Vdc2=6 V, and Vdc3=12 V—that are used in conjunction with an RL load. In contrast, the four DC voltage sources Vdc1=3 V, Vdc2=6 V, Vdc3=12 V, and Vdc4=24 V—that are used in conjunction with an RL load to generate the 31-level inverter have an analysis of 14.22% for the 31-level inverter. THD is therefore employed to lower my rising levels. For a 31-level inverter, the THD is 14.22%. A 31-level inverter improves system performance, according to the THD research. The suggested method has the most voltage boost impact and can generate more voltage levels than counterparts with the same number of switches.

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