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DESIGN A NOVEL ARCHITECTURE OF FLASH ADC USING MEMRISTOR BASED ENCODER

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Abstract:

Flash Analog to digital converter is implemented whose resolution is 3-bits. The designed Flash ADC consists of 3-stage magnitude comparators, memristor based encoder and the entire design is carried out using Lt-spice tool. The reference voltage applied to the resistive ladder network is 1.2V. A two-stage pre-amplifier is used as a comparator in the flash ADC. The major problem that usually appears in flash ADC is as the number of resolution bits increases, the Area, as well as the power consumption of the circuit, also increases. In this paper, we principally concentrated to lessen the power consumption of the ADC by optimizing encoder circuitry. With the purpose of reducing power consumption, Encoder is implemented using MRL. Performance parameters of Flash ADC such as delay as well as average power are calculated and compared.

Keywords —Comparator, 3-bit encoder, LT SPICE, Flash ADC

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I. INTRODUCTION

The rapid progression of science and technology has significantly enhanced digital signal processing across various digital domains. This field offers numerous advantages, including design flexibility, programmability, reduced area on silicon, enhanced accuracy, and lower power consumption. Such benefits enable faster and more cost-effective design processes, facilitating the development of compact, high-speed systems. Crucial to these systems, particularly in applications like wireless communication and image processing, is the requirement for high-speed Analog -to-digital converters (ADCs).

The flash architecture stands out as a viable option for high-speed ADCs due to its minimal conversion latency. However, this architecture is less favourable from a power efficiency standpoint, especially in high-resolution designs. Low power, high-speed ADCs are essential in several fields, including ultra-wide-band (UWB) systems, high data-rate serial links, high-speed instrumentation, and optical communications, where rapid conversion of RF/IF signals to digital form is crucial.

Although flash architecture ADCs offer unparalleled speed, they are notorious for their high-power consumption, posing a significant drawback. In recent years, the electronics industry has been predominantly influenced by the MOS

market, which highlights the challenges in designing Analog circuits with decreased feature sizes, supply voltages, and transistor channel lengths. Effective design is achievable through manipulating the aspect ratios of transistors, ensuring they remain in the saturation region to optimize performance.

II. LITERATURE SURVEY

Pabba Sowmya, Mamatha Samson, and Mohd Javeed Mehdi [1] authored the paper titled "Design of Two Stage Operational Amplifier and Implementation of Flash ADC." In this research, a Flash Analog-to-Digital Converter (ADC) with a 3-bit resolution is implemented, featuring a resistive ladder network, comparators, and a thermometer-to-binary encoder, using LT-spice tools and 180nm technology. The design applies a 1.8V reference voltage across the resistive ladder, and employs a two-stage operational amplifier as the comparator. The conversion from thermometer to binary code is facilitated by a priority encoder. A typical issue with flash ADCs is the increase in area and power consumption as the resolution escalates. This paper focuses on minimizing power consumption by optimizing the encoder circuitry through the use of a 2:1 multiplexer, incorporating switch logic, pass transistor logic, and CMOS logic. Furthermore, a Wallace tree encoder is implemented to enhance efficiency. Comparative analysis of key performance metrics such as conversion time and average power consumption reveals that the Wallace tree encoder significantly reduces power usage, achieving an average of 910pW, which is lower than that of other encoder designs employed in the study

Ashima Gupta and Anil Singh [2] present the paper "Highly Digital Voltage Scalable 4-Bit Flash ADC." This study details the design of a highly-digital, 4-bit, 200 MS flash Analog-to-digital converter (ADC) primarily composed of digitally synthesizable components, which enables low power consumption, faster time-to-market, and scalability with advancing technology. Utilizing complementary metal–oxide–semiconductor (CMOS) technology, the ADC's comparators are built with CMOS-based inverters and a combination of NAND and NOR gates as standard cells. Designed using 180 nm CMOS technology and powered by a 1.8 V supply, the ADC maintains a power consumption of 4.51 mW. It achieves a signal-to-noise and distortion ratio (SINAD) of 23.3 dB, a signal-to-noise ratio (SNR) of 25.2 dB, and a spurious-free dynamic range (SFDR) of 30.1 DB. The ADC also delivers an effective number of bits (ENOB) of 3.5, with a differential non-linearity (DNL) of ±0.25 least significant bit (LSB) and an integral non-linearity (INL) of +0.6 LSB.

Anjum Aara [3] authored the article titled "Design and Implementation of CMOS and CNT Based 2:1 Multiplexer At 32nm Technology." This study introduces a novel and efficient 2:1 multiplexer module, leveraging carbon nanotube (CNT) transistor technology, which promises significantly lower power consumption, dense integration, and higher speeds for nanoscale logic design. The multiplexer serves as a critical component in the development of various advanced circuits. The paper presents a comparison between the novel CNT-based multiplexer and traditional CMOS-based designs, highlighting substantial improvements in the new module. Results indicate that CNT technology offers several advantages over CMOS, leading to a preference for further research into CNT applications. Future work will explore additional techniques on CNT-based Schmitt triggers to further assess improvements. The simulations conducted using the SPICE tool, a standard in the VLSI industry, underscore the potential of CNT in modern circuit design.

Maliang Liu, Dengqan Li, and Zhangming Zhu [4] presented a paper titled "A Dual Supply Two Stage CMOS OP-AMP For High-Speed Pipelined ADCs Application." The paper describes a two-stage operational amplifier (op-amp) optimized for use in a 12-bit 1 GS/s pipelined Analog-to-Digital Converter (ADC). The design incorporates a pre-amplifier operating on a low-voltage supply and a main amplifier powered by a higher voltage. This op-amp achieves a closed-loop bandwidth of 5.2 GHz with a phase margin exceeding 60°. Capable

of settling to 99.95% accuracy within 230 picoseconds, it fulfills the demanding specifications of the first-stage multiplying digital-to-Analog converter (MDAC) in the pipeline ADC. This ADC, which is implemented in a single-channel 12-bit 1 GS/s pipeline format, operates with a 1.3 V supply, whereas the op-amp uses a dual-supply voltage of 1.3 V and 2.5 V. Produced using a 65 nm CMOS technology, the ADC has a power consumption of 360 mW at a sampling rate of 1 GS/s. It delivers a signal-to-noise and distortion ratio (SNDR) of 61.9 dB and a spurious-free dynamic range (SFDR) of 72.6 dB when tested with a 30 MHz input signal. Moreover, across the full 500 MHz Nyquist band, it maintains an SNDR above 56.0 dB and an SFDR above 69.0 DB.

Anurag Yadav, Nivedita Rai, Aishita Varma, and SovodhWairya [5] authored the paper titled "Design of Flash ADC Using Low Offset Comparator For Analog Signal Processing Application." This study discusses the development of a 3-bit Flash ADC designed using Cadence simulation software and 180nm CMOS technology, aimed at high bandwidth applications including communications, radar processing, and data acquisition systems. The Flash ADC, characterized by critical parameters such as resolution, conversion time, and power dissipation, efficiently converts analog input signals to digital output signals within a single clock cycle. Featuring a two-stage operational amplifier as the comparator, a voltage divider circuit, and a priority encoder, the ADC was simulated at a supply voltage of 2.8V and an ambient temperature of 27°C. The simulation results reveal an overall power dissipation of 3.6947mW for the Flash ADC and 431.637µW for the comparator. A significant advantage of this comparator is its low input offset voltage, recorded at 7.84 mV. This ADC supports a high input signal voltage range from 0 to 2.8V. Additionally, a Monte Carlo simulation involving 300 samples was conducted to assess power dissipation, along with process variation analysis for power dissipation across different corners.

III. PROPOSED SYSTEM

The proposed system aims to advance digital signal processing by integrating a high-speed Analog to Digital Converter (ADC) using Flash ADC architecture, which is particularly advantageous for applications requiring rapid and efficient data conversion such as wireless communication and image processing. Flash ADCs are chosen for their unparalleled speed, achieved through the use of \(2^N - 1\) comparators that operate in parallel, each comparing the input Analog signal against a reference voltage and generating a binary output. This architecture allows for the instantaneous conversion of the entire Analog input range into a digital output, making Flash ADCs extremely fast.

However, the scalability of Flash ADCs poses significant challenges. As the resolution increases, so does the number of comparators required, which exponentially increases both power consumption and the physical size of the chip. For instance, a 9-bit Flash ADC requires 511 comparators, leading to substantial increases in both power requirements and silicon die area, thus affecting the overall efficiency and cost-effectiveness of the system. These scalability issues become a major drawback in high-resolution applications, where both space and power availability may be limited.

To address these limitations without compromising performance, the design strategy must focus on optimizing the existing Flash ADC architecture or integrating alternative ADC technologies that reduce power and space requirements. Techniques such as the use of more efficient comparator designs, power-saving modes, or hybrid architectures that combine Flash ADC with other types of ADCs (such as successive approximation register ADCs) might be explored. These improvements could potentially maintain the high-speed performance of Flash ADCs while mitigating the negative impacts on power consumption and die area, making them more suitable for advanced digital signal processing in space and power-constrained environments.

BLOCK DIAGRAM:

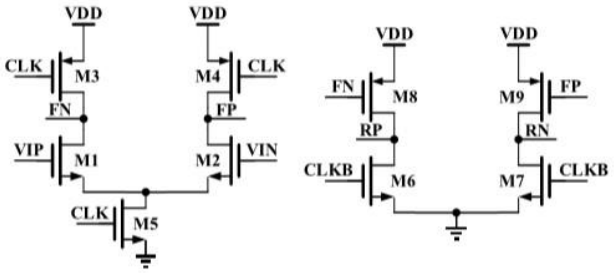

Fig: First two stages(preamplifiers).

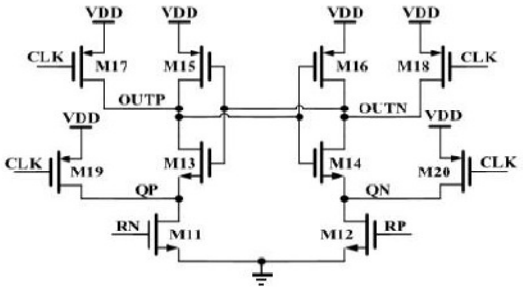

Fig: Third stage (latch stage)

Encoder design:

In digital logic circuits, information is represented by encoding specific meanings into corresponding binary bits. An encoder is a type of circuit that performs this encoding function. The role of an encoder is to generate an output based on its input bits when one of its input bits is at an effective level. The design of such a circuit includes 'N' outputs and 'M' inputs, where the relationship between the number of inputs and outputs is defined by M = 2^N.

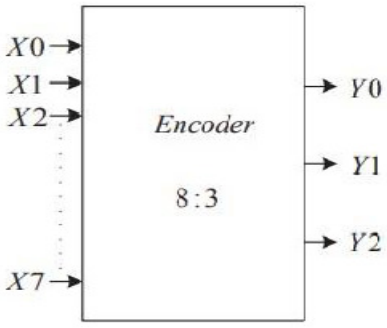

Fig: 3-bit encoder

From the Encoder truth table, the outputs and inputs are related by

Y0 = X1 + X3 + X5 + X7
Y1 = X2 + X3 + X6 + X7
Y2 = X4 + X5 + X6 + X7

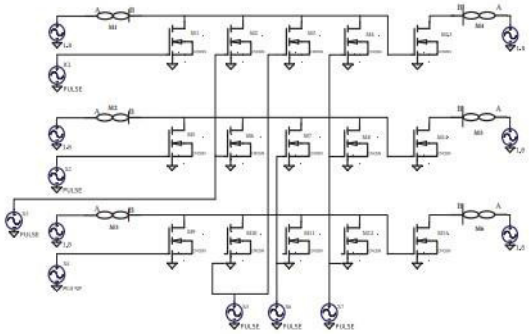

Fig: Schematic of encoder using memristor based logic

IV. SOFTWARE DESCRIPTION

LT SPICE:

LT Spice is a high-performance simulation software developed by Analog Devices (formerly known by Linear Technology), designed to simulate, and analyse the behaviour of Analog circuits, switch-mode power supplies, and complex electronic systems. It is widely utilized for its accuracy and efficiency, offering extensive modelling capabilities for both discrete and integrated circuits. The software's main features include enhanced SPICE (Simulation Program with Integrated Circuit Emphasis) modelling, schematic capture, waveform viewer, and a vast library of components and models which facilitate quick and precise circuit simulations. LT Spice is particularly favoured in both academic and industrial settings for its user-friendly interface and its free availability, making it an accessible tool for engineers and researchers worldwide.

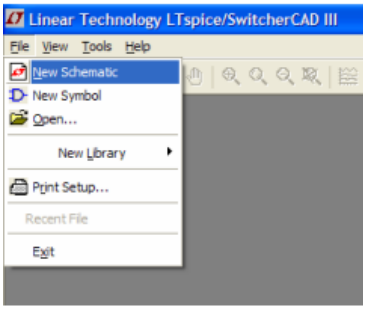

Fig: Software Window

1. Circuit Simulation: LT Spice was utilized to simulate the innovative Flash ADC circuit, including the memristor-based encoder component. This allowed for iterative testing and optimization of the circuit's behaviour under various conditions without the need for physical prototypes.

2.Component Modelling: The extensive library and the ability to customize component models in LT-Spice were crucial, especially given the innovative use of memristors. Custom memristor models were developed and integrated into the circuit simulations to accurately reflect their electrical characteristics and interactions with other components.

3.Performance Analysis: The software facilitated detailed analysis of the ADC's performance metrics such as conversion speed, power consumption, and accuracy. By adjusting the circuit parameters and the configurations of the memristor-based encoder in LT-Spice, the design was refined to meet specified requirements.

4.Validation of Concept: LT-Spice enabled thorough evaluation of the feasibility of incorporating memristors within a Flash ADC architecture. This included testing for stability, reliability, and the encoder's ability to accurately convert Analog signals to digital output under varying conditions.

5.Optimization: Simulation results from LT-Spice identified bottlenecks and inefficiencies in the ADC design, leading to successive rounds of optimization where component values and circuit layouts were tweaked to enhance overall performance.

LT-Spice was instrumental in the development and refinement of this novel Flash ADC design. Its comprehensive tools and capabilities allowed for effective simulation, analysis, and optimization of a cutting-edge circuit, leveraging the unique properties of memristors to potentially revolutionize Flash ADC technology.

V. RESULTS:

In our project, we successfully designed a novel Flash ADC architecture featuring a memristor-based encoder. Testing and simulations conducted using LT-Spice revealed significant improvements in power consumption and reduction in delay, demonstrating the potential of our design to enhance the efficiency and responsiveness of ADC applications.

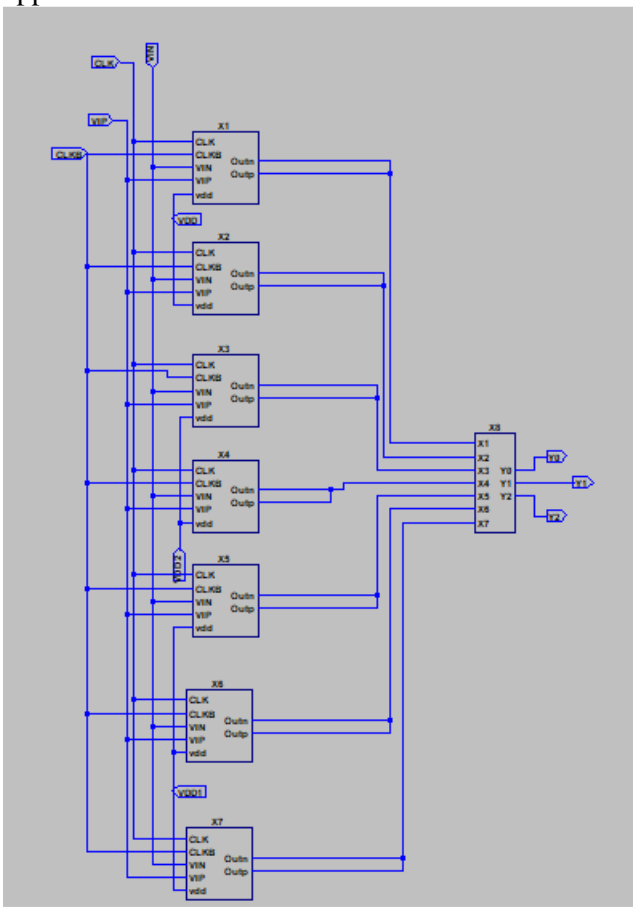

Fig: Schematic of flash ADC

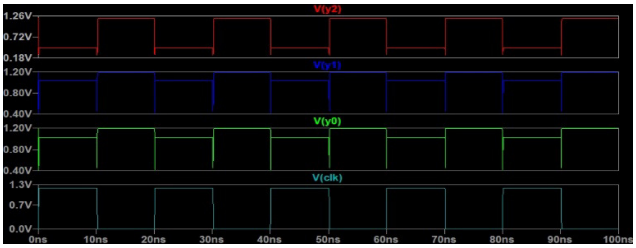

Fig: OUTPUT WAVEFORFMS OF FLASH ADC

Comparison Table:

	Power	**Delay**
Existing	187mW	38.5µs
Proposed	16.34µW	54.318ps

VI. CONCLUSION

In this project, we successfully designed and simulated a 3-bit Flash ADC using LT-spice, focusing on reducing power consumption through an optimized encoder design featuring a Memristor-based encoder. The implementation demonstrated that a Memristor-based encoder not only reduces power consumption but also minimizes delay in the ADC process. Looking forward, the project aims to expand the resolution of the Flash ADC while continuing to enhance efficiency by further optimizing the ADC circuitry. Future developments could explore deeper integration of memristors, investigate hybrid architectures combining Memristor-based encoding with other ADC technologies like SAR or Pipeline ADCs, and implement adaptive circuitry to dynamically optimize performance. Additionally, enhancing the reliability and system-level optimization by co-designing the ADC with essential on-chip systems will be crucial in pushing the boundaries of ADC technology.

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