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RESEARCH ARTICLE OPEN ACCESS

Analyzing the Performance of Space Vector Pulse Width Modulated Two and Three Level Inverter

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Abstract:

Space Vector Pulse Width Modulation (SVPWM) is an algorithm employed to regulate pulse width modulation (PWM), primarily utilized in the generation of alternating current waveforms. It finds extensive application in controlling the speed of three-phase AC motors when supplied by direct current. This research paper discusses the practical realization of two-level inverters and three-level inverters using SVPWM. When dealing with the two-level inverter eight distinct state combinations are employed to generate pulses, while the three-level inverter utilizes a total of twenty-seven switching states for the pulse generation. Additionally, the Total Harmonic Distortion (THD)is computed for both types of inverters. This implementation has been carried out using MATLAB SIMULINK.

Keywords-- **Two- level Inverter, Three- level Inverter, SVPWM, THD, SVM**

I. INTRODUCTION

Space vector modulation (SVM) is an algorithm employed to manage pulse width modulation (PWM), primarily used in the generation of alternating current (AC)waveforms. Its most common application is for controlling the speed of three-phase AC motors by varying the supplied direct current (DC)voltage. One notable area of ongoing development focuses on minimizing the total harmonic distortion (THD)produced due to the rapid switching inherent to these algorithms. Controlling the switches is crucial to prevent short circuits in the DC power supply. This can achieve by ensuring that the switches within a leg operate in a complementary manner, meeting this essential requirement.To implement space vector modulation, a reference signal can be derived from three distinct phase references using the αβ¥ transform. This paper explores, and it analyses the results of generated pulse patterns for different inverters

A. Two-level inverter using SVPWM:

The Fig. 1shows the schematic circuit of a two-level inverter consisting of six switches. Among these switches, three are upper switches, while the other switches arethe lower switches. In this configuration, it is crucial to ensure that only one switch in each leg is in the ON position, while the other switch in the same leg is in the OFF position, representing the output of the switch. We can use the binary representation, with '1' indicating an ON switch and '0' indicating an OFF switch.

Consequently, there are eight possible switch states because there are 2^3 = 8 combinations of these switches in the three legs. These statesare denoted as follows: V0 (off-off-off, V1 (off-off-on, V2 (off-on-off, V3 (off-on-on, V4 (on-off-off, V5 (on-off-on, V6 (on-on-off, and V7 (on-on-on.

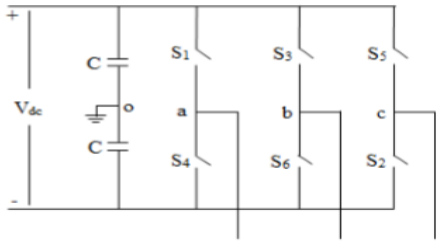

Fig. 1Schematic diagram of 3 phase 2 level inverter

In a two-level inverter, there are indeed 8 switching states.The space vector diagram depicting a two-level inverter is presented in Fig. 2. Within this diagram, you can observe six sectors, each characterized by a distinct combination of switches being either on or off in all three legs. These sectors represent the various possible states and combinations of the inverter's switches

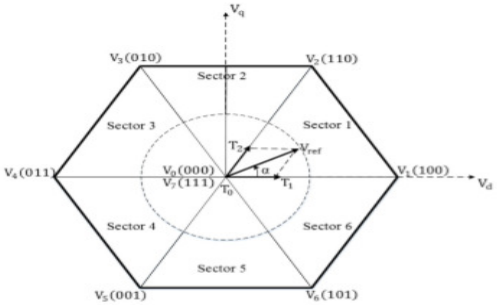

Fig. 2Inverter states and sectors of two-level inverter.

B. Three-level inverter:

In a three-level inverter, there are 12 switches, with four switches in each leg. Among these switches, bothswitches in each leg are turnedon at a time, resulting in three distinct combinations:

- When the top two switches (S1 and S2) in a leg are turned on, it is considered '0'.
- When the middle two switches (S1 and S3) in a leg are turned on, it is considered '1'.
- When the bottom two switches (S3 and S4) in a leg are turned on, it is considered '2'.

The arrangement of the switches is shown in Fig. 3. This approach allows for three different voltage levels or states to be generated in each leg of the three-level inverter, which contributes to a smoother and more precise control of the output waveform

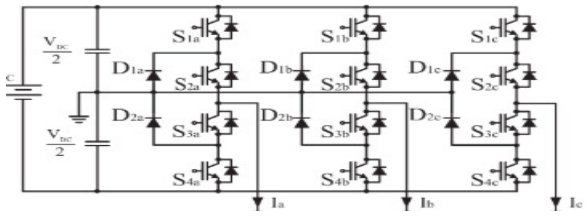

Fig. 3Visual representation ofa 3-phase 3-level inverter.

In the context of a three-level inverter, there are 27 possible switching states, each of which corresponds to a unique voltage vector. As described in [2], when the switching frequency Fs is high, the moving voltage vector Vref can be treated as stationary and it can be synthesized by carefully selecting the appropriate voltage vectors. Fig. 4consists of six sectors. Each of these sectors can be further divided into three regions or triangles. These triangular regions can be conceptually viewed as virtual two-level inverter sectors. This organization helps in understanding and controlling the inverter's output by breaking it down into smaller, more manageable sections

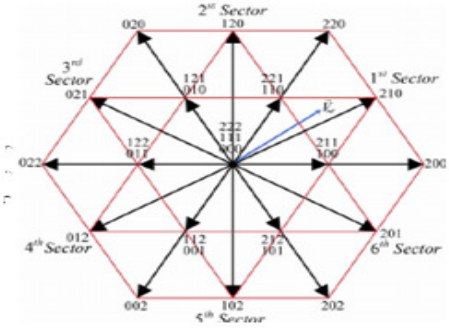

Fig. 4Inverter states and sectors of three-level inverter

II. DESCRIPTION OF THE PROPOSED WORK

This paper provides an overview of the operation of both different level inverters and discusses the utilization of SVPWM for generating pulse signals to control the switches in these inverters. The paper also presents the working principles of SVPWM as applied to both level inverters, outlining how it facilitates precise control of the output waveforms.

Furthermore, the research work is carried out using MATLAB/SIMULINK as the simulation and analysis tool. The paper specifically includes the calculation of the THD

of the load voltages for both the inverters. This analysis helps in evaluating the quality of the generated AC waveforms and assessing the operational efficiency of the inverters in terms of minimizing harmonics.

III. Simulation circuits and Results

The simulation has carried out using MATLAB/SIMULINK software and the results are discussed in this section.

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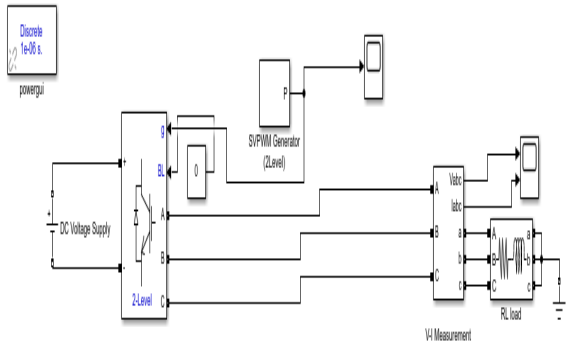

Fig. 5 Simulation circuit of a two-level inverter.

The simulation circuit for the two-level inverter employing SVPWM with an RL load is shown in Fig. 5

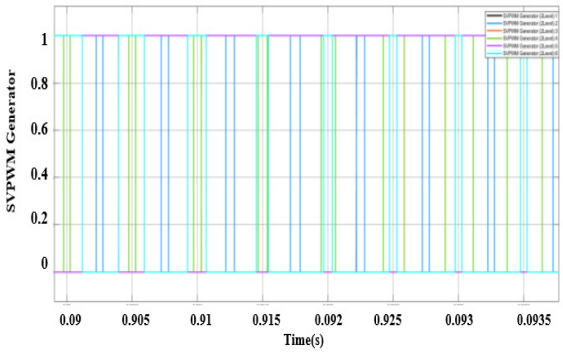

Fig. 6SVPWM pulses

Pulses are internally generated in the SVPWM block, as shown in Fig. 6

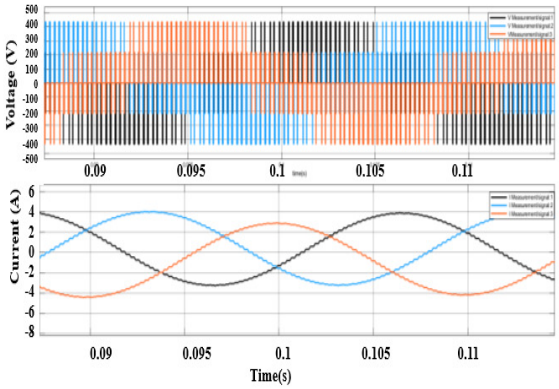

Fig. 7waveforms of voltage across the load andload current

Fig 7 shows that the voltage across the load and the current flowing through the load,when the modulation index is 0.3, the magnitude is 5A.

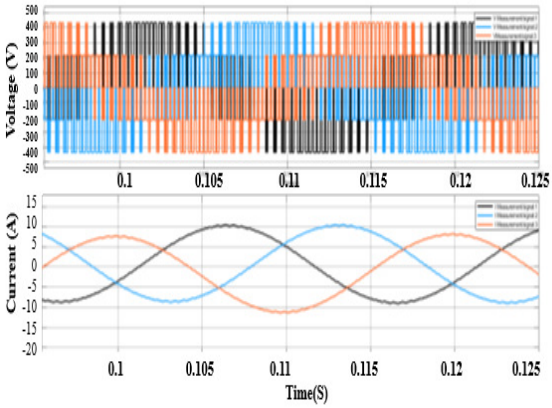

Fig. 8waveforms of voltage across the load and load current

The fig 8 shows that the voltage across the load and the current flowing through the load, when the modulation index is 0.8, the magnitude is 12A

The alteration of the modulation index results invariations in the current waveform magnitude. Changing the modulation index allows for the adjustment of the magnitude. The output voltage corresponds to the phase voltage, while the output current corresponds to the line current.

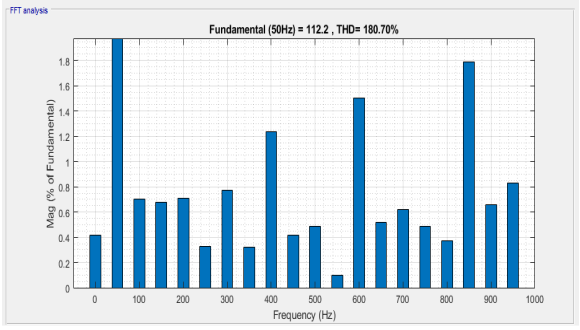

Fig. 9Voltage harmonic distortion of two-level inverter.

The Fig 9 shows that the voltage harmonic distortion of two-level inverter is the value of 180.70%

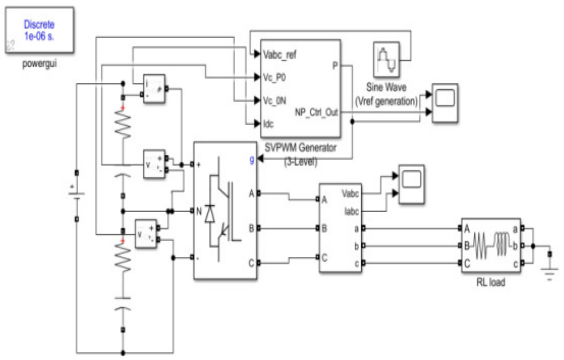

Fig. 10Three-level inverter-using SVPWM

The Fig 10 shows the simulation diagram of three level inverter using SVPWM with RL (resistive and inductive) load which is been simulated in the Simulink software.

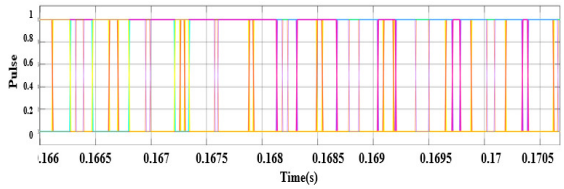

Fig. 11SVPWM pulses from the SVPWM block

The Fig 11 shows the pulses of SVPWM block used in the three level inverter.

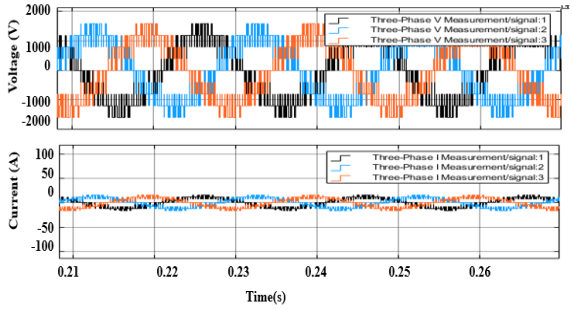

Fig. 12Output voltages and current of three-level inverter.

The Fig 12 shows that the voltage across the load and current through the load of three level inverter.

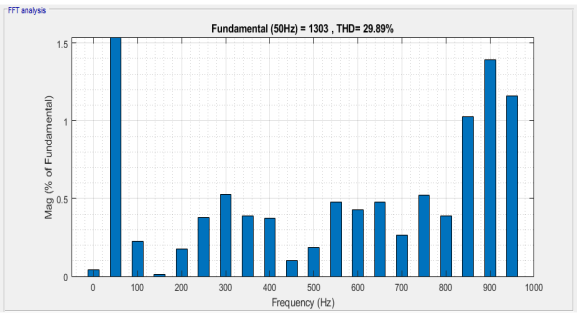

Fig. 13Voltage harmonic distortion of the three- level inverter

The Fig 13 shows that the voltage harmonic distortion of the three-level inverter is the value of 29.89%.

IV. Conclusion

The output waveforms of both two-level and three-level inverters utilizing SVPWM were analysed to discern the advantages of each. Here are the advantages of the three-level inverter

1.Improved Output Waveform Quality: The output signal waveform produced by the three-level inverter closely resembles a sinusoidal waveform, indicating a significant reduction in harmonics. This results in a cleaner and more sinusoidal output voltage.

2.Reduced Voltage Stress (Smaller V The three-level inverter exhibits a smaller voltage stress (referred to as "V" in the context of power electronics, which leads to decreased stress on the components and enhances overall reliability.

3.Voltage Clamping Diode: The presence of a clamping diode in the three-level inverter design limits the voltage during the OFF state, preventingvoltage spikes and ensuring a smoother transition between states.

Furthermore, the harmonic distortion (THD) of voltage waveforms for both inverters was calculated, and it was observed that the THD of the three-level inverter is low. This reduction in THD indicates a better quality output waveform with fewer harmonics in the three-level inverter.

These findings suggest that the three-level inverter is more advanced in terms of output waveform quality, reduced voltage stress, and lower THD. As part of future work, these techniques will be implemented in real-life applications, harnessing the benefits of the three-level inverter for practical power systems.

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