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Test-Pattern Generator in BIST- A Survey

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Abstract:

The daily advancements in VLSI technology have made chip testing more difficult. This has increased the popularity of Logic Built InSelf Test (LBIST) over Automatic Test Equipment (ATE). Logic BIST enables self-testing of chips by utilising an additional built-in hardware structure within the circuit. Test-per-scan the logic BIST structure consists of a test pattern generator, a response analyzer, a ROM, and a comparator. In a Built-in Self-Test, a test pattern generator generates a pseudorandom test pattern that can be weighted to reduce fault coverage. This paper focus on various test pattern generation methods used in BIST.

***KeyWords*:Built-in self-test (BIST), circuit under test (CUT), test-pattern generator (TPG).**

INTRODUCTION

Low-power systems for very-large-scale integration (VLSI) high-speed designs have been the focus of modern technology. As a result, several design strategies to mitigate trade-offs between performance, power, and area have been implemented. Rather than test-mode operations, several approaches have focused on low-power dissipation during BIST normal-mode operations. The switching activity in the scan chains and test data compression using the appropriate TPG are critical during BIST test mode operation.

The built-in self-test (BIST) method reduces the difficulty and complexity of VLSI testing significantly. BIST technology is broadly classified into two types: logic BIST (LBIST) and memory BIST (MBIST) [5]. The LBIST method underpins the test

pattern generation method proposed in this paper. The linear feedback shift register (LFSR)[6] generates pseudo-random test patterns in traditional LBIST technology. This results in a high test power consumption during the test.

Pseudo Random Pattern Generator

The relevant test vectors are generated by PRPG and supplied into the circuit to be tested. The LFSR is the fundamental structure that generates pseudo random patterns using a feedback polynomial. It's a type of shift register in which selected bits called taps are XORed to create a feedback polynomial that's fed to the LFSR's LSB flip-flop [4]. The internal structure of an n-bit LFSR is defined by a characteristic polynomial of degree n over GF, where coefficients reflect the presence of a feedback path. In LBIST applications, only primitive polynomials are evaluated as candidates for feedback loops since they yield the longest sequences. In the LFSR, every arithmetic operation is based on modulo 2, where multiplication is equivalent to AND and addition is equivalent to XOR.

WEIGHTED TPG

To provide acceptable statistical qualities suitable for the BIST design, the weighted TPGs are

applied in the scan chains [2]. Two approaches are used to test the BIST architecture: test-per-clock and test-per-scan. The test-point insertion method is used to test CUTs independently utilising the test-per-clock method. The method of testing the number of scan chains of the BIST in parallel is known as test-per-scan. In general, test-point insertion between scan chains can accurately provide fault coverage in the test-per-scan BIST. A TPG, response analyzer, and signature register make up the test-per-scan BIST architecture. The multiple-input signature register (MISR) is used as a response analyzer to determine whether the CUT is fault-free [7].

BMSIC-TPG

A clock management module, an original scan chain generating module, and a broadcast module make up the BMSIC-TPG structure. The clock control module (square A) is used to generate a slow clock (CLK1) and a rapid clock (CLK2) [1]. CLK1 drives the LFSR to update seed vectors, whereas CLK2 drives the rebuilt Johnson counter to update Johnson vectors and generate the vector J. The original scan chain generating module, which consists of the LFSR, the reconfigurable Johnson counter, and the exclusive OR (XOR) network, is represented by the square B. The seed vector is created using the LFSR.

The Johnson vector is generated by a reconfigurable Johnson counter, and the original scan chain vector is generated by a bitwise XOR operation of the seed vector S and the vector J by the XOR network. The broadcast module, shown by the square C, will broadcast m original scan chains to 4m broadcast scan chains[8]. To meet a target fault coverage, a small increase in test power and no increase in test length is used. The performance of the suggested BMSIC-TPG in area overhead is better for the larger CUT.

Transparent Scan

Transparent-Scan is an approach to test compactionwhere scan shift cycles and functional capture cycles areinterleaved in arbitrary ways as needed for detecting targetfaults. This work investigates the idea of using DFT logic under transparent-scan to improve test compaction without the use of additional control inputs. This is supported by the following evidence. The scan enable and scan chain input values are left unused by transparent-scan. Without any other control inputs, the unused combination can control DFT logic. Every flip-flop in the DFT logic considered in this research has a single EXCLUSIVE-OR (XOR) gate [3]. The next-state variable, as well as the scan chain input, drive the XOR gateand detailed later. The XOR gate allows the value of every next-state variable to be complemented before it is written, depending on the value of the scan chain input.

As a result, a functional capture cycle with a complemented next-state can be used to get the circuit into states required for detecting target faults in fewer clock cycles. Transparent-scan is now known as expanded transparent-scan because of the additional XOR gates.

Conclusion

This paper illustrates the various test pattern generates in VLSI testing and shows how it can be implemented in the BIST. The idea is to bringing together to illustrate as various generators to provide a test compaction and its applications in testing. This gives the clear view of how the test patterns generated during testing issuitable for all types of fault detection and diagnosis.

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