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Enhanced Data Dependent Leakage with High Speed Low Power SRAM

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Abstract:

The standard six-transistor static unpredictable access memory (SRAM) cell allows high thickness and snappy differential recognizing yet encounters half-select and read-trouble issues. Disregarding the way that the normal eight-transistor SRAM cell disentangles the examine aggravate issue, in any case it encounters low show adequacy due to disintegrating of read bit-line (RBL) swing and I on/I off extent with increase in the amount of cells per segment. Past procedures to handle these issues have been assailed by low execution, information subordinate spillage, colossal domain, and high imperativeness per find a good pace. Right now, this paper, we present three patterns of SRAM bit cells with NMOS-simply based read ports expected to unimaginably diminish information subordinate examine port spillage to enable 1k cells/RBL, improve scrutinize execution, and decrease an area and command over conventional what's increasingly, 10T cell-based works. We differentiate the proposed work and various works by account estimations from the diversion of a 128-kb SRAM worked with isolated word line-disentangling configuration what's progressively, a 32-piece word size. Beside tremendous upgrades looked out for conventional cells, up to 100-mV improvement in read-find a good pace, to 19.8% saving in essentialness per find a workable pace, to 19.5% saving in the region are furthermore observed over other 10T cells, thusly broadening the structure and application scope of memory fashioners in low-control sensors and battery-enabled contraptions.

Keywords: **10T SRAM, help techniques, E min, low force.**

I.INTRODUCTION

STATIC Random Access Memory (SRAM) has basic piece of a system on-a-chip (SoC) and has a noticeable duty to the total force use and region of the SOC. Since region is a critical factor when organizing circuits, memory arrangement Specialists plan to put indistinguishable number of cells from possible per fragment to allow sharing of periphery equipment. The conventional 6T and 8T cells are fantastic confined by their weakness to work in longer sections in light of the fact that they experience the evil impacts of data subordinate spillage and undermined ION/IOFF extent and read bit-line swing as more cells are determined to a single portion. Right now, is a need to design new circuits to address this issue. Past techniques [1]- [3] have endeavored to clarify this issue by improving the ION/IOFF extent to enable up to 1k cells per area. Regardless of the way that these techniques have been productive at this task, these still experience the evil impacts of tremendous district or fluctuating data subordinate execution. A few in like manner miss the mark to speak to the base imperativeness point in SRAMs and in this way, use a lot of essentialness for each entrance at ultra-low voltages. This work depicts three patterns of SRAM bit cells with NMOS-simply based read ports wanted to altogether lessen data ward read port spillage to enable 1k cells per RBL, improve read execution, and reduce zone and command over standard 6T and 8T cells and other novel read-port based cells. With a novel topology in all of the three cells' examined port, we get improved read find a workable pace, imperativeness per access, and low region separately, right now the structure and application go for memory makers in low control sensors and battery enabled devices. SRAM's impact has ended up being especially noteworthy because of the advancement of battery controlled helpful contraptions and low control sensor applications. Most SRAM structure effort has been provoked empower voltage scaling and improving yield. The routinely executed six transistor (6T) cell in SRAMs allows high thickness, bit-interleaving and speedy differential recognizing in any case, encounters half-select quality, read-disturb robustness, furthermore, conflicting peruse and form estimating. Past undertakings to comprehend these issues have consolidated the utilization of help systems, novel cell structure, plan improvements, or then again creative headways. Half-select and read-bother issues in SRAMs can be mitigated by progress of word-line voltage level. This fuses word-line under-drive helps using system corner following [4] or then again using propagation find a good pace. Deferred word-line help [6] to arrange within voltage of half-picked cells to that of the bit-line during a read action improves their security yet requires tweaking develop the delicate tradeoff between read security and create limit. Cell supply lift help can similarly be used to improve half-select dauntlessness by growing the drive nature of draw down NMOS Negative cell ground [7] execution to improve read strength is that the main help anyway has high vitality to utilization of various GND rails [8]. Upset issues can likewise be moderated by incomplete pre charge of bit-lines to diminish the quality of access transistors [9] utilize controllers to lessen the pre charge voltage level of the bit-lines to around 70% of supply voltage to improve the read soundness. On the other hand, the bit-line filter be pre charged utilizing a NMOS rather than a PMOS to get a solitary VTH drop on the bit-lines [10]. A procedure variety tolerant specific pre charge help [11] has likewise been utilized to diminish bit-line voltage level exploitation charge sharing to improve half-select upset issues. Be that as it may, such halfway piece line pre charge strategies diminish read capacity and become less powerful at lower voltages because of decreased VDS of the entrance transistors. Numerous stockpile line help can likewise be utilized to improve peruse and compose half-select strength issues in SRAMs. In [12], a segment based powerful stockpile strategy was proposed. By executing distinctive inventory voltages for read, compose and backup modes, it assuaged half-select dependability issues and permitted bit-interleaving. Be that as it may, this brought about increment in unique force, structure and directing exertion and region because of age of numerous stockpile voltages. In spite of the fact that help procedures can be gainful in improving the exhibition and yield of SRAMs, they can frequently have a falling apart integral impact on compose and read activities. They can

likewise acquire huge territory overhead, increment the vitality per get to, and have a constrained and immersing impact on yield. Besides, since peruse and compose strength is enormously reliant on temperature varieties, a SRAM can either be compose constrained at lower temperatures or read-restricted at higher temperatures. Hence, helps regularly require procedure and temperature following for compelling yield improvement. Aside from help procedures, enhancements for the engineering front have furthermore been made to deal with half-select and read upset soundness issues. These incorporate cross-point choice of words utilizing both line and segment word-lines to improve half select security. Shorter piece lines can likewise be utilized to improve read soundness. These work by decreasing piece line capacitance, accordingly improving unique read edge. In any case, this comes to the detriment of huge territory overhead because of more noteworthy number of cell banks. In another work, a cluster design with a territory overhead of 12% was actualized so as to address the half-select upset issue by decoupling the enormous piece line capacitance from half-chose cells. Peruse and-compose back plan [3] has likewise been utilized to lighten the compose upset into equal parts select cells. It permits information maintenance by composing back the put away information after each read. Nonetheless, such strategies increment the dynamic force utilization since each section is exposed to full voltage swings. For sure, the sense electronic gear can't be shared among numerous segments and must be coordinated in every section, along these lines causing an enormous territory overhead. With the 6T SRAM cell being tormented by different solidness issues, the 8T SRAM cell has been arranged (appeared in Fig. 1). It has a decoupled perused way including two NMOS transistors. in spite of the fact that it dispenses with the read-upset issue, it is as yet bugged by a pseudo-read during a make action into equal parts picked cells on a comparative section. In that limit, the issue of loss of bit-interleaving limit rises Bit-interleaving is essential to low voltage SRAM action since it is merged with Error-Correction Code (ECC) to fight fragile mix-ups and achieve required yield targets. Fragile errors, including Single Bit Upsets (SBUs) and Multiple Cell Upsets (MCUs) are achieved by flood of alpha-particles, warm neutrons or of course high imperativeness immense shafts. The pace of fragile botches augments by 18% for each 10% decrease in stock voltage. Additionally, bit-interleaving capable cell structures, for example, the area decoupled 8T. Still irritated by a pseudo-read during a create action into equal parts picked cells on a comparable segment. In that limit, the issue of loss of bit-interleaving limit rises. Bit-interleaving is fundamental to low voltage SRAM movement since it is solidified with Error-Correction Code (ECC) to fight sensitive mix-ups and achieve required yield targets. Fragile errors, including Single Bit Upsets (SBUs) and Multiple Cell Upsets (MCUs) are realized by flood of alpha-particles, warm neutrons or on the other hand high essentialness huge bars. The pace of fragile bumbles augments by 18% for each 10% decrease in stock voltage. This is especially precarious for low voltage SRAMs, since in sub-limit action region, the essential charge in center points is in a general sense diminished, inciting ordinary MCUs. MCUs have been directed by completing and solidifying bit-interleaving structure with ECC. Additionally, bit-interleaving capable cell structures, for example, the segment decoupled 8T cell. Trouble free 9T cell., two-port aggravate free 9T cell, multi-port 9T cell, and the differential 10T cell have been proposed to enable piece interleaving and remove half-select trouble issues by using both line and fragment word-lines. For cell structures without interleaving limit, for instance, the single completed 8T cell, additional uniformity or ECC bits can be interleaved per word for sensitive misstep amendment. Whether or not the peruse and form bother issues are helped using the procedures portrayed more than, a display executed using the 8T cells has low group efficiency. This is since, its single completed instrument requires a dynamic identifying plan which realizes as not many as eight cells for each area RBL and distinctive close by RBLs per overall RBL. Also, as opposed to the fast differential identifying in the 6T cell, the single got done with recognizing has a moderate full swing action. As increasingly conspicuous number of cells are put on a comparable neighborhood RBL .in order to improve show profitability, both deferment and the read bit-line voltage swing are altogether impacted. In this manner, this kind of different leveled recognizing doesn't approach differential identifying similar to both execution and show efficiency. Yet various techniques have been proposed to improve the single completed readidentifying execution, the area overhead despite everything remains tremendous. In order to improve the bunch capability what's more, read bit-line voltage swing of single-completed read cells, many changed read ports have been proposed [1]-[3].

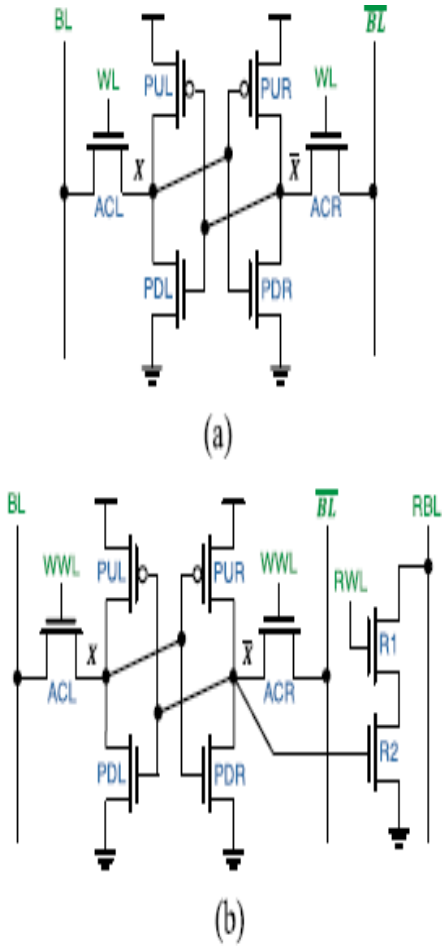

Fig. 1(a). Schematic of 6T and (b) schematic of 8T

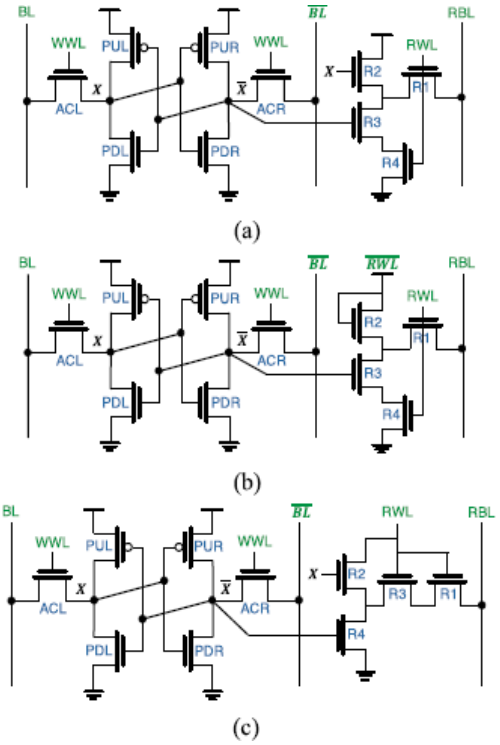

Fig. 2. Schematic of the proposed (a) 10T-P1, (b) 10T-P3, (c) 10T-P2 cells

These structures intend to set up to 1k cells per bit-line by improving the ION/IOFF extent of SRAM read ports. This philosophy serves to exceptionally improve the bunch capability as periphery equipment can be shared among progressively important number of cells. In spite of the way that these techniques have been productive at this task, these still experience the evil impacts of gigantic zone, moving data subordinate execution what's increasingly, high imperativeness usage. Right now, propose three accentuations of SRAM bit cells with NMOS-simply based scrutinize ports and differentiation them and conventional 6T and 8T cells and past 10T cell-based works by evaluating estimations from reenactment of a 128kb group on the 32nm development center. We process least essentialness per access for all phones considering unmistakable development factors for various degrees of stores and discover dynamic frustration rate reliant on working repeat and method assortments. The paper has been worked as seeks after. Section II depicts the proposed cells and their working standard and Segment III fuses the introduction evaluation of various piece cells dependent on read bit-line swing, essentialness per find a workable pace, probability and zone. Portion IV compresses what's more, shuts the paper.

1. PROPOSED SRAM BITCELL

A. Topology of proposed bitcells

The schematic of the proposed 10T SRAM cells is showed up in Fig. 2. All of them includes cross coupled inverters (PUL-PDL and PUR-PDR) and two access transistors (ACL and ACR). The read port of each cell involves four NMOS (R1, R2, R3 and R4). The read port in Fig. 2(a) has improved data ward read bit-line spillage and is pointed at first class. The read ports in Fig. 2(b) and (c) have absolute data self-governing examined bit-line spillage and are away for low force and high thickness exclusively. The working of each port has been explained in the accompanying fragmentin enormity between found a workable pace in the two cases. Taking everything into account, a basic fruitful RBL swing can be viewed. This is past the domain of creative

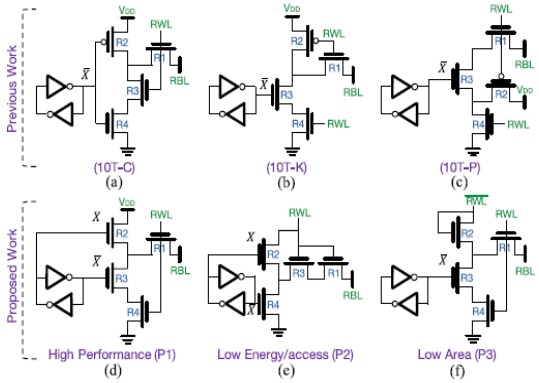

Fig. 3 Schematic of read port of (a) Calhoun and Chandrakasan [1], (b) Kim *et al*. [3], (c) Pasandi and Fakhraie [2], (d) Proposed 10T-P1, (e) 10T-P2,(f) 10T-P3 cell.

B. Bit Cell WorkingMechanism

When working right up front and sub-edge zone, the Particle/IOFF is truly spoiled and it ends up being logically difficult to complete progressively significant number of cells on a lone segment. As the amount of cells increase, the joined leave door spillage finishes behind identical to the read current, right now great speaker to precisely survey the read bit-line voltage level. In addition, the data set aside in the cell also impacts the read bit-line spillage hence making the off-state read bit-line spillage current to differ particularly. This is exacerbated at ultra-low voltages, where the most negative situation data model can provoke the RBL voltage level of 'zero' finding a good pace unmistakable than the RBL voltage level of 'one'. In order to improve the ION/IOFF extent, the read port showed up in Fig. 3(a) was proposed in [1]. Right when the cell stores 'one,' the R2 PMOS charges the midway center, right now diminishing the read bit-line spillage through R1 NMOS. In any case, this also prompts stream of spillage current from center into the RBL. The joined spillage of all cells on a comparative section can raise the low reason level of RBL to two or three hundred mV, thusly inciting diminished voltage swing and distinguishing edge. The sensible circumstance of the amazing examined bit-line voltage swing. On the other hand, when the cell stores 'zero,' the RBL spillage is lessened through the stacking effect of NMOS. Along these lines, such a topology makes the feasible RBL swing, as it were, subject to the data plan in the segment. In another work [3], the data dependence was emptied by making a data free spillage route between the cell examine port and the RBL. This provoked a gigantic voltage swing on the RBL even at lower voltages. The read port what's more, the looking at fruitful RBL swing for the proportionate has been showed up in Fig. 3(b). A continuous work [2], in like manner proposed a changed read port [shown in Fig. 3 (c)], to improve the ION/IOFF extent. Regardless, it is excessively troubled by the data subordinate spillage way issue. Contingent on the data set aside in the phone, the spillage from widely appealing center point to RBL can change profoundly, thusly provoking fluctuating low basis voltage levels of RBL. Notwithstanding this issue, it is competent to keep up a RBL swing. From here on, the cells in Fig. 3(a), (b) and (c) will be implied as the 10T-C, 10T-K and 10T-P cells independently. Like the proposed cells, these cells moreover have a

comparative topology for the make port and differ the extent that the read port so to speak. The schematic of the proposed read ports is showed up in Fig. 3(d)– (f). The proposed 10T-P2 and 10T-P3 cells are pointed at low force and low area independently while at the same time keeping up a data free ION/IOFF extent. The standard behind their working is depicted. The significance of I spill ends up equal in both read 'zero' and read 'one' case. This keeps up the necessary qualification in enormity between found a workable pace in the two cases. Taking everything into account, a basic fruitful RBL swing can be viewed. This is past the domain of creative mind in the case of customary 8T cell distinguishing, because of the colossal dependence of spillage current on the data plan. Regardless of the way that the proposed 10T-P1 cell reduces its data dependence interestingly with the 10T-C cell. It, all things considered, remains unequipped for playing out a read action at ultra-low voltages. Regardless, in the going with subsection, we exhibit that working at ultra-low voltages manufactures the imperativeness per access and working near the edge point is perfect for most insignificant essentialness use. Taking everything into account, the 10T-P1 cell is worked near as far as possible region for most decreased imperativeness use and best. At close restrict and super-edge voltages, the read bit-line swing isn't an issue for the 10T-P1 cell. A continuously broad assessment of RBL.

2. EVALUATION OF SRAMCELLS

A. ClusterDesign

To check the presentation of proposed cells and break down them with past works, we executed a 128kb bunch using each cell. Since all of the phones which have been pondered are slanted to create madden issue, the bunch was worked in a non-interleaved designing without segment select equipment. The show contains four 32kb sub-discourages each with 1024 cells for each segment and a 32-piece word size. Rapid Limited Switch Dynamic Logic (LSDL) was utilized to assemble the pre decoders and decoders. Ten area bits were used as commitments to make sixty-four NOR based pre decoders, whose yields were then used as self-arranged pulses to drive the decoder-driver for each line. Different leveled-Word-Decoding (HWD) realizes lower control use likewise, faster access time interestingly with Divided-Word line-Deciphering (DWD). This is because the HWD configuration realizes additional degrees of word-lines to lessen the general capacitance per line select way. In any case, the good conditions are inconsequential for more diminutive groups (< 256kb). Since as far as possible is simply 128kb, the DWD plan was used. Specific pre charge using BS (Block-Select) was used to engage the pre charge of bit-lines of simply the found a workable pace lessen dynamic force usage. Four metal layers were used to course VDD, GND, bit-lines besides, the close by and overall word-lines. The transistor evaluating for all cells contemplated right now showed up in Table 1. The proposed 10T-P1 cell, with its remarkable topology and configuration, had the alternative to manufacture the evaluating of R3 NMOS, thusly provoking huge updates in read execution. While this change didn't immediate an extension in the district of cell, it brought about fairly extended hold control.

Table 1
Transistor width sizing
(nm)

DESIGN	ENERGY	AREA
10T SRAM USING PMOS	25.8%	28.6%
10T SRAM USING NMOS	19.8%	19.6

While close by RWLs and WWLs were completed in each push for all cells, the RWL for the 10T-P3 cell was shared among two touching lines. Such a use was made as a result of the limited vertical pitch of every section and the wiring need of a couple of level neighborhood and overall lines in each push. At whatever point a read action is played out, the RWL goes to low level for two sections. Regardless of the way that the spillage current from the half-picked segment grows, the general augmentation in IOFF for each RBL is almost no and doesn't influence read execution. The arranging diagram for the memory movement. The WL (word-line), RD (read) and WR (make) are sure edge synchronized with the clock signal. Both the close by RWL and WWL are engaged with the negative edge of clock signal. The WL is gotten together with the yield of each pre decoder to enable new location disentangling, exactly toward the beginning of each movement. The bit-lines are pre charged toward the beginning of each create movement, after which the data is stacked onto them before the engaging of WWL. Likewise, all the local piece lines of the found a workable pace overall RBLs are pre charged during the fundamental part of the read clock cycle. The RWL is enabled during the second half of the clock to allow the RBL to develop prohibitively. The voltage level on the RBL is perceived by the sense speaker, which is at that point used to survey the overall RBL. The DIDO (Data-In-Data-Out) produces cognizant yield as showed by overall RBL level.

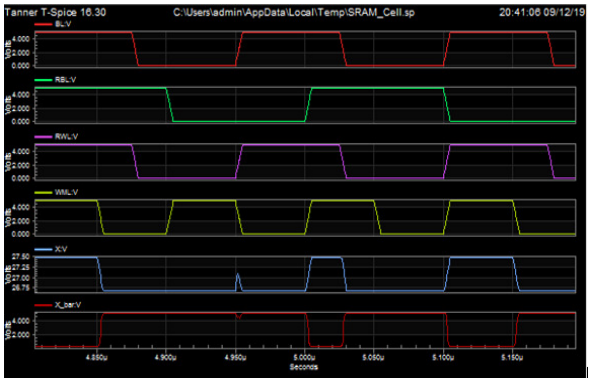

Fig. 4. Results

B. *Peruse Bit-LineSwing*

When playing out a read movement, a satisfactory read edge is required for right evaluation by the sense enhancer. This edge is ensured by a tremendous RBL swing, which is ideally the qualification among VDD and GND. Regardless, the joined spillage from all cells into the RBL or from RBL into the cells, can truly degenerate the low and high method of reasoning levels independently, right now diminished edge for right distinguishing at lower voltages. The disintegrating in RBL swing is moreover exacerbated at higher temperatures as a result of augmentation in spillage current. On

occasion, the RBL swing is moreover affected by the data subordinate spillage path in the read ports of SRAM cells. The effective RBL swing, as a degree of VDD, and with respect to contrasting voltage, temperature and data configuration is showed up for all cells. The accompanying three cases have been seen as while assessing the RBL swing –

1) All cells in the segment store 'zero.'

2) All cells in the segment store 'one.'

3) 'One' and 'zero' are passed on correspondingly in the fragment.

As found in Fig. 8, the 10T-C cell's fruitful RBL swing is generally negligible among all cells contemplated and moves inconceivably consenting to the data structure. The 10T-K cell has a data self-sufficient spillage route in its read port, which prompts a data self-governing RBL swing. The 10T-P cell in like manner has a data subordinate RBL swing, yet with a lower level of assortment. The feasible RBL swing in the proposed 10T-P1 cell has a much lower dependence on the data configuration interestingly with the 10T-C cell. Regardless of the way that it is data subordinate, it is away for first class what's increasingly, close/super-limit action, where RBL swing isn't an issue. Both the 10T-P2 and 10T-P3 cells have an information autonomous RBL swing, with the 10T-P2 showing the most raised RBL swing.

C. Reserve LeakagePower

At some irregular voltage and temperature, the complete force of the cell should be as low as would be judicious. As needs be, a complete connection of typical save spillage control per cell as to voltage, temperature and data structure assortments. The going with three cases have been pondered while evaluating reinforcement control

1) All cells in the show store 'zero.'

2) All cells in the show store 'one.'

3) 'One' and 'zero' are passed on also.

The proposed cells use least spillage control interestingly with past work all things considered voltages and temperatures. It can in like manner be watched that a comparable movement of 'zero' and 'one' data prompts the most skeptical situation spillage control if there ought to be an event of 10T-C, 10T-P, 10T-P1 moreover, 10T-P2 cells. The 10T-K and 10T-P3 generally have the most significant spillage control when they store 'zero.' However, this example doesn't keep up over all stock voltages and temperatures. The 10T-P2 cell, which eats up most negligible force right up front and sub-edge territory, has a startling augmentation in power usage at higher voltages in view of addition in stream of passage tunneling spillage current. At 27°C, the 10T-P3 cell goes from eating up lower control than the 10T-C cell in super-edge district to higher force use in sub-limit region. In spite of the way that this example stays steady at lower temperatures (−10°C) as well, at high temperatures (80°C), the 10T-P3 cell reliably The supreme force is also affected by the repeat of movement, trading activity, design ward interconnect supply voltage. Since all phones considered right now basic differentiations in interconnect wiring because of changing point of view extents, the total unique force will moreover vacillate colossally. In this manner, in the accompanying subsection we evaluate the total imperativeness per access for all cells.

3. SIMULATIONRESULTS

To check the presentation of proposed cells and think them with past works, we realized a 128kb group using each cell. Since all of the cells which have been broke down are slanted to form trouble issue, the bunch was created in a non-interleaved plan without area select equipment. The group contains four 32kb sub-prevents each with 1024 cells for each area and a 32-piece word size. Rapid Limited Switch Dynamic Logic (LSDL) was utilized to fabricate the pre decoders and decoders. Ten area bits were used as commitments to make sixty-four NOR based pre-decoders, whose yields were then used as self-arranged pulses to drive the decoder-driver for every segment. Different leveled-Word-Decoding (HWD) realizes lower control usage likewise, speedier access time conversely with Divided-Word line-Deciphering (DWD). This is in light of the fact that the HWD building executes additional degrees of word-lines to lessen The general capacitance per segment select way.

4. CONCLUSION

Right now, showed three strengths express read ports with improved data free read port spillage for SRAM cells went for prevalent, low force and low locale exclusively. Every one of the three proposed read ports didn't execute any PMOS, thusly inciting more diminutive n-well size, which consequently provoked humbler vertical estimating and shorter piece lines in the petite structure positions. This reduced the region per cell and imperativeness per find a good pace. All of the SRAM cells with the proposed scrutinize ports improved the fruitful read bit-line voltage swing what's progressively, enabled 1k cells per read bit-line, allowing uncommon potential for zone saving similarly as sharing periphery equipment. With a unique topology in all of the three cells' scrutinized port, we get a best-case find a workable pace 483mV for the 10T-P1 cell, an E min of 7.19pJ/acc for the 10T-P2 cell, and a low region of 0.55728μm2 for the 10T-P3 cell. In assessment to normal cells, this causes an understanding of to up to 180mV improvement in read to find a workable pace up to various occasions decline in essentialness per access at their individual V min. Right when stood out from past 10T cell-based works, about 100mV improvement in read find a good pace, to 19.8% saving in imperativeness per find a good pace, to 19.5% saving in district can be viewed, right now the structure and application run for memory originators in low force sensors and battery enabled devices.

REFERENCES

[1] B. H. Calhoun and A. P. Chandrakasan, “A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation,” *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 680–688, Mar.2007.

[2] G.PasandiandS.M.Fakhraie,“A256-kb9Tnear-thresholdSRAMwith 1kcellsperbitlineandenhancedwriteandreadoperations,”*IEEETrans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2438–2446, Nov.2015.

[3] T.-H.Kim,J.Liu,J.Keane,andC.H.Kim,“A0.2V,480kbsubthreshold SRAM with 1 k cells per bitline for ultra-low-voltage computing,”*IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 518 529 Feb. 2008.

[4] V. P.-H. Hu, M.-L. Fan, P. Su, and C.-T. Chuang, “Analysis ofGeOIFinFET 6T SRAM cells with variation-tolerant WLUD read-assist and TVC write-assist,” *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1710–1715, Jun.2015.

[5] S. Ohbayashi*et al.*, “A 65-nm SoC embedded 6T-SRAM designed for manufacturability with read and write operation

stabilizing circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 820–829, Apr.2007.

[6] M.E.Sinangil,H.Mair,andA.P.Chandrakasan,"A28nmhigh-density 6TSRAMwithoptimizedperipheral-assistcircuitsforoperationdownto 0.6V,"in*IEEEInt.Solid-StateCircuitsConf.(ISSCC)Dig.Tech.Papers*, Feb. 2011, pp.260–262.

[7] M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, Y. Nakase, andH. Shinohara, "A 45 nm 0.6 V cross-point 8T SRAM with negativebiased read/write assist," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2009, pp. 158–159.

[8] B.Zimmer*etal.*,"SRAMassisttechniquesforoperationinawidevolt age range in 28-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 12, pp. 853–857, Dec.2012.

[9] H.Pilo*etal.*,"A64MbSRAMin32nmhigh-*k*metalgateSOItechnology with 0.7 V operation enabled by stability, writability and read-ability enhancements," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 97–106, Jan.2012.

[10] A. J. Bhavnagarwala*et al.*, "A sub-600-mV, fluctuation tolerant 65-nm CMOS SRAM array with dynamic cell biasing," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 946–955, Apr.2008.

[11] M. H. Abu-Rahma, M. Anis, and S. S. Yoon, "A robust single supply voltage SRAM read assist technique using selective precharge," in *Proc. 34th Eur. Solid-State Circuits Conf.*, 2008, pp.234–237.

[12] D. Anh-Tuan, J. Y. S. Low, J. Y. L. Low, Z.-H. Kong X. Tan, and K.-S. Yeo, "An 8T differential SRAM with improved noise margin for bit-interleavingin65nmCMOS,"*IEEETrans.CircuitsSyst.I,Reg.Papers*, vol. 58, no. 6, pp. 1252–1263, Jun.2011.

