RESEARCH ARTICLE OPEN ACCESS

Study of power consumption in 7T SRAMS CELL for Future inhencement in CMOS

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Abstract:

The objective of this report is to describe the power consumption of a 7T-transistor SRAM cell. The basic operation and constraints of static RAM will be discussed, along with transistor sizing for device stability. The design will be covered using a symbolic schematic, as well as a physical device layout (both generated using Electric VLSI Design System). To demonstrate that this 6T SRAM cell design operates correctly for all four necessary functions: write HIGH, write LOW, read HIGH, and read LOW. The basic purpose of a memory cell is to hold a single bit of data, and this can be accomplished statically (without the need for refreshing) by using a pair of inverting gates. In order to read from and write to this invertor pair, access transistors are also needed.

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I. INTRODUCTION

In CMOS devices, the current deep-sub nano meter technology with low threshold voltages, sub threshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. The leakage power is becoming significant component of the total power and may contribute to majority of the power dissipation in future CMOS technologies. The two main sources of power dissipation in CMOS circuits are dynamic power dissipation and static power dissipation. Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bi-stable latching circuitry made of Transistors MOSFETS to store each bit. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops. The power is most important factor for today technology so the power reduction for one cell is vital role in memory design techniques. In this paper we introduced some design circuit techniques for low power design. Leakage current in standby mode is the major part of power loss. We concentrate on the technique that to reduced the leakage current in standby mode. The one CMOS transistor leakage current due to various parameter is the vital role of power consumption.7T SRAM cell and 7T SRAM cell-1 are compared in terms of their power consumption, delay and SNMs Power comparison between novel 7T SRAM cell and 7T. The increase in leakage current is an important factor of CMOS device.

II. LITERATURE SURVEY

The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled to each other with additional NMOS Transistor which connected to read line and having two pass NMOS transistors connected to bit linesand bit-lines bar respectively. Low power memory is required today most priority with also high stability. The power is most important factor for today technology so the power reduction for one cell is vital role in memory design techniques. In this paper we introduced

some design circuit techniques for low power design. Leakage current in standby mode is the major part of power loss. We concentrate on the technique that to reduced the leakage current in standby mode. The one CMOS transistor leakage current due to various parameter is the vital role of power consumption. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method. The circuit level technique is reduced power consumption at very high level. In this paper we simulate the 7T SRAM cell using many techniques both circuit level, process level in one cell as Hybrid cell. All transistors have minimum length (L_{MIN} =45nm according to used Technology), while their widths are typically design parameters. The value of W_{P1} and W_{P2} defines PMOS transistors width and W_{N1} and W_{N2} defines the NMOS driver transistors width use in CMOS Invertors, while W_{N3} and W_{N4} is the access.

III. SEVEN TRANSISTOR 7TSRAM CELL

This type of RAM is one of the most common, due to its low leakage and compactness. A downside of the 6T SRAM is the need of more external circuitry to perform read and write operations, but when many memory cells are used with only one read and write driver for the whole grid, this is a good tradeoff.The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled to each other with additional NMOS Transistor which connected to read line and having two pass NMOS transistors connected to bit linesand bit-lines bar respectively.The access transistors MN3 is connected to the word-line (WL) to perform the access write and MN4 is connected to the Read-line (R) to perform the read operations thought the column bit-lines (BL and BLB). Bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write in the memory cells during write operations. All transistors have minimum length (L_{MIN} =45nm according to used Technology), while their widths are typically design parameters. The value of W_{P1} and W_{P2} defines PMOS transistors width and W_{N1} and W_{N2} defines the NMOS driver transistors width use in CMOS Invertors, while W_{N3} and W_{N4} is the access transistors width.Leakage current occurs in both active and standby modes. It is recommended to switch off the leakage current when the circuit is in standby mode. Drain and source to well junctions are typically reverse

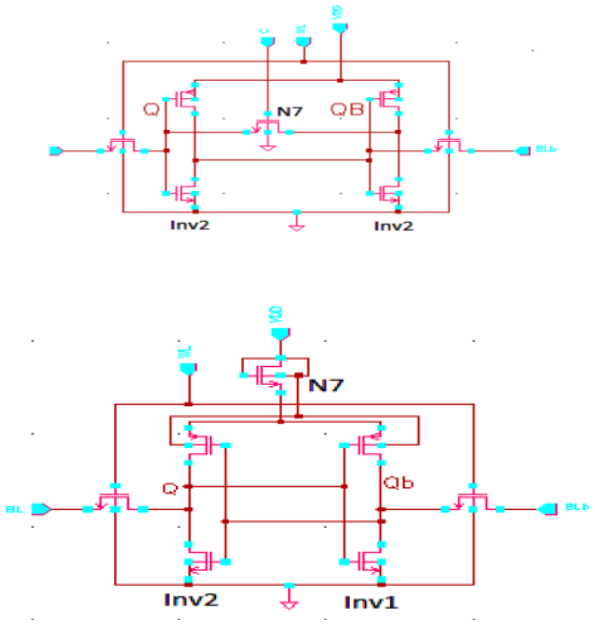

Fig 1

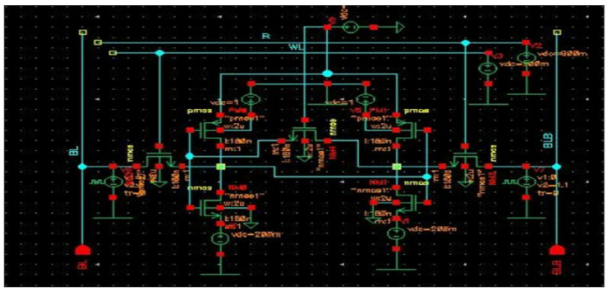

Fig2 7T SRAM DESIGN

IV. POWER CONSUMPTION IN SRAM CELL 7 T

The one CMOS transistor leakage current due to various parameter is the vital role of power consumption. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method. The circuit level technique is reduced power consumption at very high level. The Sub threshold is the drain-source current of a transistor operating in the weak inversion
region. Leakage current occurs in both active and tandby modes. It is recommended to switch off the leakage current when the circuit is in standby mode. Main objective of proposing this new 7T SRAM cell is to have good Read Stability and Static Noise Margins. Fig 5. Static and Dynamic power trends
The circuit of 7T SRAM cell is made of two CMOS inverters that connected to cross coupled to each other with additional NMOS Transistor which connected to read line and having two pass NMOS transistors connected to bit lines and bit-lines bar.
In CMOS SRAMs there are two important. To fulfill this objective using two supplies to allow the SRAM to run in two different modes. Nominal supply voltage is used for powering of the peripheral circuits as decoders. , the leakage current is becoming a major contributor to the total power consumption. In current deep-sub nanometer technology with low threshold voltages, sub threshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. The two main sources of power dissipation in CMOS circuits are dynamic power dissipation and static power dissipation. Static power dissipation is due to leakage current when the transistor is normally off. The improvement in technology scaling has introduced very large sub threshold leakage current, therefore careful design techniques are very important in order to reduce sub threshold leakage current for low power design. Leakage current occurs in both active and standby modes. It is recommended to switch off the leakage current when the circuit is in standby mode.Various result of current and power

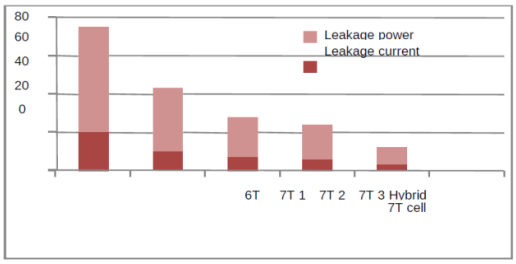

FIG 3

V.COMPARISION OF POWER CONSUMPTION IN 7T FROM 6T

The power comparison between novel 7T SRAM cell and 7T SRAM cell-2. 7T SRAM cell consumes more power compared to 7T SRAM cell-2 but 7TSRAM cell-2 lacks in good SNMs .The cellwhich has small SNMs is more susceptible for noises and don't ensure the protection of data. Therefore 7T SRAM cell-2 design is not a good SRAM cell design. Comparison with Previous Work: Performance comparison with previous memory cells in several aspects such as access time, static noise margin, and power consumption are presented. comprises of regular CMOS inverter pair to hold the data whereas ST-1, ST-2, ST11T and proposed design (ST13T) utilizes Schmitttrigger inverter pair. As we know that differential bit cells accomplish very less access time over single ended designs, so that the conventional 6T cell takes less time as 0.5 ns and 0.1 ns to write 1 and 0 into the memory cell at the supply voltage of 0.4 V with 22nm technology. In contrast to this, ST11T bit cell utilizes the virtual ground technique to reduce the write-1 access time: however, due to the single ended methodology ST11T offers high write-1 access time than the 6T cell, 7.5ns at supply voltage of 0.4 V with 22nm technology.

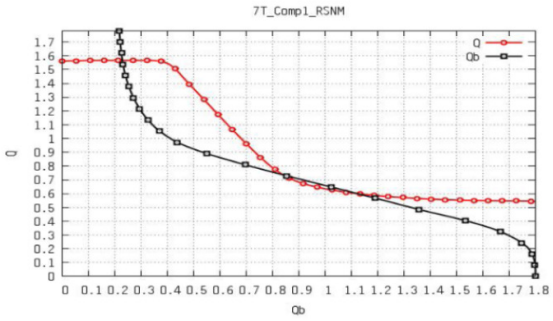

Fig 4

CONCLUSION:

In this paper power dissipation of 6T SRAM is compared with 7T SRAM. Simulation and analysis of 6T SRAM and 7T SRAM is desired. Simulation result shows clearly how read and write operation is performed. It is observed that the power dissipation is less as compared with 6T SRAM to the 7T SRAM in read as well as write mode of operation. In future, power dissipation will play a major role to reduced

ACKNOWLEDGMENT

Affirmation The creators are grateful to Mr. Aseem Chauhan (Additional President RBEF, Chancellor AUR), Maj. General K. K. Ohri, AVSM (Retd.), Pro Vice Chancellor, AUUP, Lucknow Campus and Wing Cd (Dr) Anil Kumar Tiwari (Director, ASET) for their participation, inspiration and suggestive direction.

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