An Energy Efficient Design of Hybrid CMOS Full Adder

Mrs. M VIJAYA LAKSHMI *,K CHARAN KUMAR **, C ANIL ***, D HIMABINDU ****,

M BHARADWAJ *****,S CHINNARAJU******

(Associate Prof, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India)1

(B.Tech. IV Year Student, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India) 2
(B.Tech. IV Year Student, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India) 3
(B.Tech. IV Year Student, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India) 4
(B.Tech. IV Year Student, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India) 5
(B.Tech. IV Year Student, ECE Dept, Siddartha institute of science and Technology, Puttur, A.P, India) 6
(Email.id: -kakkecharan21@gmail.com)

Abstract:

This article explores the principles, applications, advantages, and challenges of Transmission Gate Based Modified Gate Diffusion Input (TGMGDI) circuits, a novel approach in digital circuit design. TGMGDI builds upon the Gate Diffusion Input (GDI) technique by integrating transmission gates to enhance performance, reduce power consumption, and improve scalability. Leveraging transmission gates' bidirectional switching capabilities, TGMGDI circuits offer faster switching speeds, lower propagation delays, and improved noise immunity compared to traditional GDI implementations. Overall, TGMGDI represents a promising advancement in digital circuit design, with ongoing research aimed at furthering its adoption and integration into next-generation digital systems.

Keywords — GDI, TGMGDI, Hybrid CMOS, Full Adder.

I. INTRODUCTION

The introduction provides background information before delving into the ideas, uses, and difficulties of Transmission Gate Based Modified Gate Diffusion Input (TGMGDI) circuits and digital circuit design. TGMGDI is a new method that combines GDI with transmission gates to increase performance and reduce power consumption. This is especially useful in fields like microprocessor design and digital signal Examining processing. how TGMGDI developments can transform the field of circuit design, this study hopes to shed light on how it integrates with new technologies and how it might influence the development of digital systems that will be used in the future.

Within VLSI technology, the Gate Diffusion Input (GDI) method is a promising path toward reduced circuit complexity and increased power

efficiency. Because GDI reduces the number of transistors in logic circuits and minimizes power consumption during transitions, it is a versatile solution that may be used in a wide range of applications, from safety-critical equipment to personal computers. Its versatility highlights how crucial a position it plays in advancing electronics advancement by guaranteeing compactness, performance, dependability, and affordability for a wide range of electronic systems.

The TGMGDI system is a noteworthy progression of the GDI methodology, using transmission gates to enhance signal transfer and reduce leakage current. By adding transmission gates, TGMGDI aims to improve the performance and flexibility of GDI-based designs, with the potential to improve noise immunity, reduce power consumption, and facilitate effective signal propagation in digital circuits. This breakthrough could pave the way for more effective and highperforming circuit designs by meeting the changing needs of contemporary digital systems.

methods, backed by comparisons with previous methods and actual findings.

II. LITERATURE SURVEY

Bhuvaneshwari, Dhanushya, Gayathri, and Kavitha's [1] "Low Power CMOS GDI Full-adder Design," explores innovative techniques in digital circuit design to address power consumption challenges in full-adder circuits using the Gate Diffusion Input (GDI) methodology. The authors propose novel modifications to traditional CMOS designs, leveraging GDI to enhance power efficiency while maintaining performance. By integrating GDI techniques, the proposed full-adder design achieves reduced transistor count and improved switching characteristics. The paper discusses the theoretical framework behind GDIbased circuits and presents detailed simulation results to validate the effectiveness of the proposed design approach. Additionally, the authors highlight the potential applications of their design in lowpower computing systems and digital signal processing. Overall, the study contributes valuable insights into the development of energy-efficient digital circuits, with implications for various fields of electronic engineering.

M. K. Roberts, P. Anguraj, and T. Krishnan [2] "Design and Analysis of Improved Low Power and High-Speed N-Bit Adder. "The study explores the crucial area of digital circuitry and offers a thorough analysis of cutting-edge methods for improving the effectiveness and performance of Nbit adder circuits. The authors present innovative methods that solve power consumption and speed limits through careful design and thorough analysis. Their research highlights the importance of adder circuits in modern computer systems and clarifies the effects of improved designs in a range of applications, including signal processing, microprocessor architecture, and arithmetic operations. Using cutting-edge techniques and modelling tools, the authors provide insightful analysis of the trade-offs that arise in adder design between power, speed, and area. The study also offers a thorough examination of the suggested

"A Unique Design of Hybrid Full Adder for the Application of Low Power VLSI Circuits," S. S. Singh, D. Leishangthem, M. N. Shah, and B. Shougaijam [3] introduce a novel hybrid full adder design tailored for low-power VLSI circuits. This innovative design integrates multiple logic models to maintain high performance while minimizing power consumption. Through rigorous analysis and simulation. demonstrate the authors the effectiveness their of approach without compromising speed or area efficiency. Their study not only elucidates the intricacies of full adder implementation but also offers valuable insights into achieving low power in VLSI circuits. With potential applications in microprocessor design, digital signal processing, and energy-efficient computing, this research represents a significant advancement in low-power VLSI architecture with far-reaching implications for next-generation electronic devices.

C. S. Manikandababu, M. Jagadeeswari, and S. Manju [4] "Accuracy Reconfigurable Adder for Low Power of Sobel Edge Detection Algorithm." This study delves into low-power circuit design and image processing, aiming to develop reconfigurable adder tailored for the Sobel edge detection algorithm. The authors propose an adder architecture capable of adjusting its accuracy to the specific requirements of edge detection tasks while minimizing power consumption through innovative circuit design techniques. By optimizing resource utilization in edge detection applications, this approach contributes to the advancement of energyefficient image processing systems.

H. Seo, Y. S. Yang, and Y. Kim [5] explore the realm of energy-efficient adder designs with their paper titled "An Energy-Efficient Imprecise Adder with a Lower-part Constant Approximation." Their project aims to develop an imperfect yet energyefficient adder architecture with a tolerable level of precision. Introducing a novel approach, the authors employ constant approximation techniques in the lower half of the adder to reduce energy

International Journal of Scientific Research and Engineering Development-– Volume 7 Issue 2, Mar-Apr 2024 Available at www.ijsred.com

consumption in arithmetic operations. Through extensive simulations, Seo et al. demonstrate the effectiveness of their inaccurate adder design in achieving significant energy savings compared to conventional architectures. The paper underscores the importance of balancing energy efficiency and accuracy and discusses the trade-offs between the two. With potential applications in embedded systems, Internet of Things devices, and mobile computing, this research provides valuable insights into creating energy-efficient arithmetic units for low-power computing environments. Furthermore, it offers strategies for enhancing inaccurate adder designs and integrating them into computing settings with energy constraints.

III. PROPOSED SYSTEM

The integrates proposed system Transmission Gate Based Modified Gate Diffusion Input (TGMGDI), a cutting-edge technique poised to enhance efficiency and performance in digital circuit design. By leveraging transmission gates within the GDI structure, TGMGDI offers superior signal propagation, reduced leakage current, and enhanced noise immunity compared to conventional GDI implementations. Operating on the same principles as traditional GDI circuits, TGMGDI introduces bidirectional switches via transmission gates, enabling signals to pass with minimal voltage drop and propagation delay. This innovation promises higher speed, lower power consumption, and improved robustness, making it ideal for a diverse range of applications spanning digital signal processing, microprocessor design, communication systems, and low-power electronics. Another notable advantage of TGMGDI lies in its enhanced noise immunity. The bidirectional switches provided by transmission gates contribute to a robust signal integrity, minimizing the susceptibility to external interference and ensuring reliable operation even in noisy environmentsa critical requirement in applications such as wireless communication systems and high-speed data processing.The proposed system harnesses TGMGDI's potential to revolutionize circuit design,

paving the way for more energy-efficient and highperformance digital systems.

BLOCK DIAGRAM:

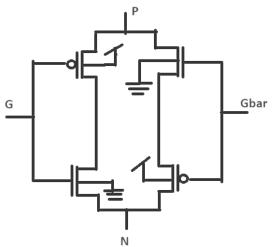


Fig: TGMGDI Cell structure

Principles of Operation:

At its core, TGMGDI operates on the same principles as traditional GDI circuits, employing a combination of NMOS and PMOS transistors to implement logic functions. However, the inclusion of transmission gates introduces additional functionality and versatility to the design. Transmission gates act as bidirectional switches, allowing signals to pass through in both directions with minimal voltage drop and propagation delay.

N	Р	G	Output	Function
0	Y	А	X'Y	F1
Y	1	Х	X'-Y	F2
1	Y	Х	X+Y	OR
Y	0	Х	X.Y	AND
Z	Y	X	X'Y+XZ	MUX
0	1	Х	X'	NOT
Y'	Y	X	X'Y+XY'	XOR
Y	Y'	X	XY+X'Y'	XNOR

This capability enables TGMGDI circuits to achieve higher speed, lower power consumption, and improved robustness compared to conventional GDI implementations.

IV. SOFTWARE DESCRIPTION CADENCE EDA:

International Journal of Scientific Research and Engineering Development-– Volume 7 Issue 2, Mar-Apr 2024 Available at www.ijsred.com

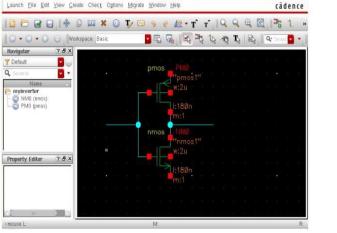
The following Cadence CAD tools will be used in this tutorial:

- Virtuoso Schematic for schematic capture.
- Spectre for simulation.
- We will practice using CADENCE with a CMOS Inverter: creating (1) Schematic (2) Simulation.

Computer Account Setup: ENVIRONMENT SET UP FOR CADENCE AND ADDITIONAL TOOLS

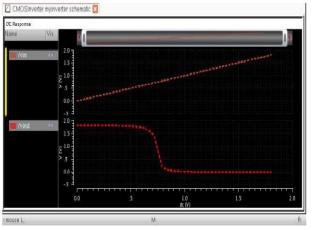
Steps To Create New Project: >>mkdir cadence >>cd cadence Now start Cadence by typing >>csh >> source cshrc >>cd cadence_ms_labs_613 >>virtuoso



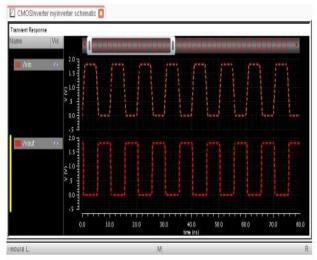


Virtuoso® Schematic Editor L Editing: CMOSInverter myInverter schematic



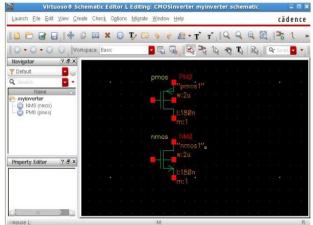


Simulation Results (DC analysis)



Simulation Results (Transient Analysis)

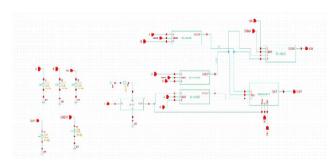
Terminal window



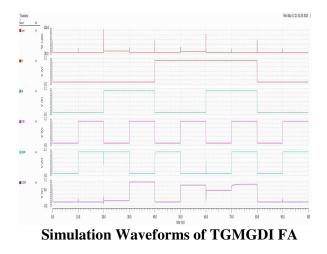
NMOS and PMOS on schematic

International Journal of Scientific Research and Engineering Development-– Volume 7 Issue 2, Mar-Apr 2024 Available at www.ijsred.com

V. RESULTS:



Schematic of the proposed TGMGDI FA



Launch Session Setup	<u>A</u> nalyses	Variables	Outputs Sin	nulation <u>R</u> esul	ts <u>I</u> ools	Calibre	Help	cāde	e n o
127) 👌 ≻	• 👌 🖥	1 🗁						
esign Variables			Analyses					75	×.
Design Variables Name Value Iran ⊻ 0 10Cn moderate									
			Outputs (7)					× (
				Signal/Expr	Value	Plot	Save	Save Options	T
		- 11	1 A			2	<u> </u>	ally	- 1
			2 D 3 CIN			× ×		ally	1
			4 SUM			Ĵ.	5	ally	
			5 COUT			Ū.	ū	allv	
		- 10	6 total power		5.8317Gu				
		- 10	7 delay betwe	en sum and cin	-5.69365p				
			8 delay betwo	en cout and cin	-3.72763p				
		- 11		ulation: Auto				Replace 🔽	

Area, Power, Delay Reports

S.NO	Parameters	Existed Method	Proposed Method		
1	Power	14.184 µw	5.8317 µw		
2	Delay Between Sum and cin	3.982 ps	-5.69365 ps		
3	Delay Between cout and cin	-2.483ps	-3.72763 ps		

Table: Difference Between Existed and proposed method

VI. CONCLUSION

To sum up, research into Transmission Gate Based Modified Gate Diffusion Input (TGMGDI) is an important step in improving digital circuit performance and energy economy. design's TGMGDI provides better noise immunity, lower power consumption, and improved signal propagation by fusing transmission gates with the GDI structure. This novel technique has potential electronics. applications low-power in microprocessor design, and digital signal processing. We expect additional improvements in speed, reliability, and resource efficiency as we develop and apply TGMGDI methodologies, ushering in a new era of energy-efficient digital systems.TGMGDI has the potential to shape the future landscape of digital electronics, enabling transformative solutions that enhance our quality of life while minimizing our environmental footprint. As we continue to explore the capabilities of TGMGDI, we move closer to realizing a vision of a more sustainable and technologically advanced society.

VII. FUTURE SCOPE

We The Transmission Gate Based Modified Gate Diffusion Input (TGMGDI) circuits, as described in the article, present an exciting avenue for digital circuit design. Let's delve into the future scope and potential modifications for this novel approach:

Advanced Applications:

Microprocessor Design:As microprocessors continue to evolve, integrating TGMGDI circuits could enhance their performance. These circuits

International Journal of Scientific Research and Engineering Development-- Volume 7 Issue 2, Mar-Apr 2024 Available at www.ijsred.com

cancontribute to efficient arithmetic operations, cache design, and memory access.

Low-Power Electronics:TGMGDI's power-saving features make it appealing for low-power devices, such as wearables, IoT sensors, and battery-operated gadgets.

Emerging **Technologies**: Investigate how TGMGDI synergize with emerging can technologies like quantum computing, neuromorphic computing, or reversible logic gates. These intersections may lead to groundbreaking innovations.

VIII.REFERENCES

- Bhuvaneshwari, Dhanushya, Gayathri, Kavitha, "Low Power CMOS GDI Full-adder Design," 2023 9th International Conference on Advanced computing and communications Systems (ICACCS) 2023 IEEE DOI:1109/ICACCS57279.2023.10112885.
- M. K. Roberts, P. Anguraj and T. Krishnan, "Design and Analysis of Improved Low Power and High-Speed N-Bit Adder," 2021 International Conference on Decision Aid Sciences and Application (DASA), 2021, pp. 858-863, doi: 10.1100/DASA53625.2021.0682405

10.1109/DASA53625.2021.9682405

- S. S. Singh, D. Leishangthem, M. N. Shah and B. Shougaijam, "A Unique Design of Hybrid Full Adder for the Application of Low Power VLSI Circuits," 2020 4th International Conference on Electronics, Communication and AerospaceTechnology (ICECA), 2020, pp. 260-264, doi: 10.1109/ICECA49313.2020.9297594.
- 4. C. S. Manikandababu, M. Jagadeeswari and S. Manju, "Accuracy Reconfigurable Adder for Low Power of Sobel Edge Detection Algorithm," 2021.
- 5. H. Seo, Y. S. Yang and Y. Kim, "An Energy-Efficient Imprecise Adder with a Lower-part Constant Approximation," 2020 International SoC Design Conference (ISOCC), 2020, pp. 143-144, doi: 10.1109/ISOCC50952.2020.9332922.
- 6. M. Keerthana and T. Ravichandran, "Implementation of Low Power 1-bit Hybrid Full Adder using 22 nm CMOS Technology," 2020 6th International Conference on Advanced

Computing andCommunication Systems (ICACCS), 2020, pp. 1215-1217, doi: 10.1109/ICACCS48705.2020.9074256.

- J.Cho and Y. Kim, "Low Power Approximate Multiplier Using Error Tolerant Adder," 2020 International SoC Design Conference (ISOCC), 2020, pp. 298-299, doi: 10.1109/ISOCC50952.2020.9332952.
- [8] S. A. Simon and S. S, "Implementation of Carry Save Adder Using Novel Eighteen Transistor Hybrid Full Adder," 2020 International Conference on Power Electronics and Renewable Energy Applications (PEREA), 2020, pp. 1-4 4, DOI: 10.1109/PEREA51218.2020.9339799.
- B. Shankar, S. N. Gupta, P. Tiwari, M. K. Ojha and D. Gupta, "Low power adder using multi gate FET in 32nm technology," 2022 2nd International Conference on Advance Computing and Innovative Technologies in Engineering (ICACITE), 2022, pp. 1576-1579, doi: 10.1109/ICACITE53722.2022.9823595.
- 10. K. A. Maniusha, B. Naresh, D. Subodh and K. Sahithya, "Low Power and Area Efficieny ALU With Different Type of Low Power in Full Adders," 2021 Asian Conference on Innovation in Technology (ASIANCON), 2021, pp.1-6, doi:10.1109/ASIANCON51346.2021.9544561.