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Total Harmonic Reduction in Cascaded Based Switched Capacitor Multilevel Inverter with Reduced Components

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Abstract:

The purpose of the paper's abstract is to develop a switched capacitor multi-level inverter that produces voltages higher than the input direct current voltage. In this research, we investigate the various multi-level inverter techniques for lowering switching frequency and total harmonic distortion (THD) voltage in the inverter's bus output, hence increasing the overall efficiency of the multilevel inverter. Additionally, this inverter can reduce the requirement for an output side transformer or capacitors, as well as the input step up dc voltage converter system is needed. The primary goal is to lessen the gap between the two in order to cancel out the net error voltage and quality of the power output is improved. The performance is enhanced overall while size and expense are decreased. To demonstrate the performance of the new topology, a comparison with classic topology is conducted in terms of switches used, DC sources used, diodes, output power quality, and THD attained.

Keywords — Switched capacitor multilevel inverter, THD, Selective Harmonic Elimination

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I. INTRODUCTION

Due to their great characteristics in terms of high power capacity, low switching voltage stress, low harmonics, modular and scalable design, MULTILEVEL inverters (MLIs) play a significant role in power electronics systems [1]. Electric vehicles (EVs), renewable energy systems, and flexible ac transmission networks all make extensive use of multilevel inverters (MLIs). All areas of electrical engineering, including renewable energy conversion, high voltage DC transmission, distributed generation (DG) systems, contemporary drive applications, uninterruptible power supplies, and others, use MLIs extensively [2]. The conventional topologies of neutral point clamping (NPC), flying capacitors (FC), and cascade H-bridges (CHB) have been thoroughly investigated and used in a variety of applications. The increased number of components, capacitor voltage balancing, and sophisticated control for a higher number of levels [3] have been the problems with these inverters, nevertheless. They need a lot of power switches and clamping devices in traditional MLIs such cascaded h-bridges, neutral point clamped, and flying capacitor types, which raises the weight, size, and losses.

In [4], a lower number of power switches with a switched capacitor topology is advised in order to prevent using many active switches. But the highest output voltage, which is applied to the switches in these topologies, causes them to experience severe voltage stress. Different SCMLI topologies are provided for various output voltage levels in [5] in order to reduce the severe stress on the switches.

Since each of the SC units can operate in a bipolar fashion in the suggested topology, the high stage of voltage unfolding is avoided. Each unit is capable of simultaneously providing both positive and negative voltages while performing capacitor recharge during every cycle [6]. Low- and medium-power applications are best suited for the SCs-based MLIs. The suggested inverter's output harmonics are additionally lessened by the use of multi carrier PWM approaches.

With dc input supply voltage, the switched capacitors in SCMLI are designed in series and parallel for charging and discharging respectively. Additionally, the complexity of the control of system is reduced by SC based topologies with capacitors that balance their own voltage without the use of any auxiliary techniques. The inverter has the capacity to step up voltage and can produce multilayer voltage from a dc source.

II. PROPOSED CASCADED MULTILEVEL INVERTER

A. Circuit Topology

This multilevel inverter uses PWM techniques with high switching frequencies and passive filters at the output terminals to improve the harmonic spectrum and THD. Two capacitors (C1 & C2) are strategically positioned to increase output voltage levels while stepping up voltage magnitude with fewer parts. The DSC MLI is also developed using eleven unidirectional blocking directional conducting switches and one bidirectional blocking directional conducting switch.

The two capacitors are needed to provide a output voltage level of Vdc/2, which causes the staircase voltage of the output waveforms to be less than Vdc. This effectively lowers total harmonic distortion (THD) in the output voltage. The Switched capacitor circuit, which provide series-parallel conversion between the power source and capacitors and produces the step voltage level, is made up of switches S5, S6, S7, S8, S9, and capacitors C1, C2.

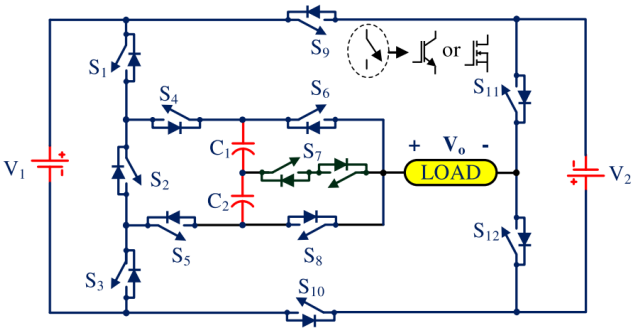

Fig 1. Circuit diagram of 9 level SCMLI

The switches S1 and S2 are used to switch on and off between the voltage sources of 0.5V & V to display at the output, and the switch S3 can be used to get the two input sources of voltage sum. S3 and S4 in this circuit are utilized to charge the capacitors to a level of the voltage 2Vdc. When the output voltage level Vin is synthesized, the input source also supplies energy to the load, thus the parallel charging of the capacitors continues. The system size is reduced by the suggested inverter's lack of inductors. The output sources for the suggested inverter can be capacitors, batteries, and other dc voltage sources. The suggested inverter may provide nine level step waveform thanks to the collaboration of the switches: 2Vdc,3Vdc/2,Vdc, and 0.

B. Modulation Strategy

A variety of modulation techniques, including phase disposition pulse width modulation (PD-PWM), selective harmonic elimination (SHE)

PWM, third harmonic injection (THI) PWM, and others, can be utilized for MLIs. The suggested nine-level topology is driven by the selective harmonic elimination (SHE) technique to provide a output voltage waveform with high quality content and switching frequency of the inverter is low.

The SHE approach can particularly reduce the harmonics content in the output waveform and lower the output voltage's THD by choosing the switching device's conducting angle. Even though the loss acquired by the switching is minimized and the frequency level is kept constant, the Selective harmonic elimination control approach is a widely used various switching strategy for MLIs. By analysing a particular fitness function, the intended lower harmonics described by a set of harmonic content in the output equations can be removed. This approach is based on resolving a particular objective function by doing a Fourier series analysis on the output voltage waveform.

Consequently, the voltage Vo of the fourier decomposition is analysed by

$$V_{o=}\ \frac{2V_{dc}}{\pi}\sum_{k=1,3,..}^{\infty}\sum_{i=1}^{4}\frac{\cos(k\theta_i)}{k}\sin(k\omega t) \quad (1)$$

According to the analysis of waveform synthesis, the output voltage can be expressed as

$$V_o = \sum_{i=1}^{4} V_{oi}$$

Thus, the output voltage Vo of the fourier decomposition is given by

$$V_{o=}\ \frac{2V_{dc}}{\pi}\sum_{k=1,3..}^{\infty}\sum_{i=1}^{4}\frac{\cos(k\theta_i)}{k}\sin(k\theta t) \quad (2)$$

The amplitude modulation index M_{of} is expressed as

$$M_{of} = \frac{1}{4}\sum_{i=1}^{4} cos\theta_i \quad (3)$$

The output waveform's THD is provided by

$$\text{THD} = \frac{\sqrt{\sum_{k=3,5..}^{\infty}[\sum_{i=1}^{4}\cos(k\theta_i)]}}{\sum_{i=1}^{4} cos\theta_i}\ 100\% \quad (4)$$

C. State Analysis

Below table lists the various inverters operating states, including on control and off control states of inverter switches, and capacitor charging and discharging states. It is obvious that 1 and 0 represent the ON and OFF functioning of switches, while "C", "D", and "-" stand for the charging, discharging, and idle states of capacitors, respectively. The voltages of the series capacitors C1 and C2 are naturally maintained at 0.5Vdc and Vdc, respectively, without the use of any sophisticated control mechanisms or supplementary balance circuits. To achieve the ideal capacitance value, the longest discharge time (LDT) of each of the capacitor for one cycle of output voltage at sustainable frequency is required.

Table I
Operating states of the proposed inverter

State	Switches											Capacitor		Output levels
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	C_1	C_2	
1	1	0	0	1	0	1	1	0	0	0	0	D	D	$2V_{dc}$
2	1	0	0	1	0	1	0	1	0	0	0	D	_	$3\frac{V_{dc}}{2}$
3	1	0	0	1	0	0	0	0	1	0	0	C	C	V_{dc}
4	0	0	0	1	0	0	0	0	1	1	1	C	D	$V_{dc}/2$
5	0	1	0	1	0	0	0	0	1	0	0	C	C	0
6	0	0	1	0	0	0	0	0	1	1	1	D	C	$-V_{dc}/$
7	0	1	1	0	0	0	0	0	1	0	0	C	C	$-V_{dc}$
8	0	1	1	0	1	0	1	0	0	0	0	_	D	$-3\frac{V_{dc}}{2}$
9	0	1	1	0	0	1	1	0	0	0	0	D	D	$-2V_{dc}$

When the switches Sw3, Sw5, Sw6, Sw8, Sw9, Sw10, and Sw11 are turned ON or OFF, respectively, the voltage levels +Vs or -Vs are produced. The capacitor C1, which has a voltage Vs, is linked with DC voltage source in series at the voltage levels +Vs and -Vs. The further SCs C2 are linked in series. The series combination created by the parallel combination of DC voltage source and the capacitor C1 by this series string.

D. Capacitance Analysis

1. Capacitance Voltage Balance Analysis

The discharging cycle for each capacitor should be taken into consider while choosing the appropriate number for used capacitors in the inverter circuit. The basic switching, in which the LDC occurs in the both of the half-cycles yield voltage waveform

for C1 and C2, respectively, is what causes the 9-level voltage of the developed inverter to be formed in the output.. The maximum discharging capacity of each capacitor during LDC is obtained from

$$Q_c = 2\times \int_{t_6}^{\frac{T}{2}-t_6} I_L(t)\, dt \qquad (5)$$

energy in the capacitors; this cycle is repeated. The continuous discharge value of Ci over its Each capacitor's biggest voltage ripple occurs during its longest discharging period. Actually, throughout this time, the load is receiving the longest discharging duration will be determined as follows, assuming the load is a pure resistor.

$$\Delta Q_i = \int_{t_{ai}}^{t_{bi}} \sqrt{2} I_L \sin(2\pi f_0 t)\, dt \qquad (6)$$

Therefore, the capacitance of C(i)should be chosen as

$$C_i > \frac{\Delta Q_i}{\Delta V_i}$$

Capacitor voltage imbalance will cause output voltage bias, which will result in overvoltage, over current, capacitor breakdown, etc., which will instantaneously cause the system to fail. The load has no bearing on the charging time or current. Two capacitors are directly linked to a dc source in the charging stage, which allows the capacitor voltage to quickly achieve the rated value. Thus the capacitor C1 discharge amount in one cycle is

$$\Delta Q_1 = \frac{1}{2\pi f_o}\left(\int_{\theta_3}^{\pi-\theta_3} i_o\, d\omega t + \int_{\pi+\theta_1}^{\pi+\theta_2} i_o d\omega t + \int_{\pi+\theta_4}^{2\pi-\theta_4} i_o d\omega t + \int_{2\pi-\theta_2}^{2\pi-\theta_1} i_0\, d\omega t\right)$$

where , f_o is the fundamental frequency, and ω is the angular frequency of the output voltage.

The discharging amount of capacitor C1 is

$$\Delta Q = \frac{V_{dc}}{2\pi f_0 R_0}(4\pi - \theta_1 + \theta_2 + 3\theta_3 - 5\theta_4) \qquad (7)$$

Therefore, Capacitor C_2 discharging amount in one cycle is

$$\Delta Q_2 = \frac{1}{2\pi f_o}\left(\int_{\theta_1}^{\theta_2} i_o\, d\omega t + \int_{\theta_4}^{\pi-\theta_4} i_o\, d\omega t + \int_{\pi-\theta_2}^{\pi-\theta_1} i_o\, d\omega t + \int_{\pi+\theta_3}^{2\pi-\theta_3} i_0\, d\omega t\right)$$

2. Selection of Capacitor Value

By providing the input dc supply in parallel combination, capacitor C3 charges up during the output negative voltage half cycle at zero voltage levels and -Vdc. The time constant RC for the charging loop has a value that is less than the charging period. The capacitor C2 is fully charged as a result. The energy available in the capacitor is transmitted to the output at voltage levels of 1.5Vdc and 2Vdc. The voltage in the capacitor, or ripple voltage, falls as the level of stored energy declines instantly. The recommended selection of the capacitor's capacitance value, which is given by, can control the ripple voltage.

$$C = \frac{I_{pk}}{\Delta V_c \times f_0} \qquad (8)$$

where I_{pk} is the maximum load current, ΔVc is the unwanted harmonic voltage and fo is the output voltage frequency.

3. Capacitor Determination Analysis

During LDTs, the same number of charges (i.e.,QC1 and QC2) are discharged from C1 and C2. Where t3, t4 are the voltage level transition durations and Ci is the capacitor current during LDT. The formula for t3 and t4 can be shown below when using the basic switching frequency modulation approach.

$$\Delta Q_{c1} = \Delta Q_{c2} = \Delta Q = \int_{t_3}^{\frac{T}{2}-t_3} i_C dt \qquad (9)$$

The capacitor's discharging current during LDTs is equivalent to the I_o current. Now, assuming a R_o load and a fundamental output frequency of 50 Hz, it is possible to assess the volume of charges during LDTs by

$$\Delta Q_{c1} = \Delta Q_{c2} = \Delta Q = \frac{2V_{dc}}{R} \times 0.0103$$

Capacitor C2 can discharge continuously up to $[\pi+\theta_3,\ 2\pi-\theta_3]$, and the discharge current is still equal to the load current i0. Capacitors C1 and C2 have the same maximum continuous discharging interval and associated functioning condition. Only the capacitor C1 is estimated for ease of analysis. The formula for C1's maximum discharge amount is given by

$$\Delta Q = \frac{1}{2\pi f_0} \int_{\theta_3}^{\pi-\theta_3} i_o \, d\omega t \quad (10)$$

Therefore, using in j×V as the peak value for each capacitor's voltage harmonics, the ideal capacitance for each capacitors may be expressed as follows.

$$C_{op} = \frac{Q_{ci}}{j \times V_{in}}$$

Additional calculation of the maximum continuous discharging amount ΔQ include

$$\Delta Q = \frac{1}{2\pi f_0}\left[\int_{\theta_3}^{\theta_4} \frac{3V_{dc}}{2R} \, d\omega t + \int_{\theta_4}^{\pi-\theta_4} \frac{2V_{dc}}{R} \, d\omega t + \int_{\pi-\theta_4}^{\pi-\theta_3} \frac{3V_{dc}}{R} \, d\omega t\right] \quad (11)$$

In the interval [θ3, θ4] and [π - θ4, π - θ3], the voltage V_o is 3Vdc/2. In the interval [θ4, π- θ4], the voltage V_o of the inverter is 2Vdc. Therefore, the maximum continuous dissipated charge is

$$\Delta Q = \frac{V_{dc}(2\pi - 3\theta_3 - \theta_4)}{2\pi f_0 R_0} \quad (12)$$

According to the design rule, the harmonic voltage should not exceed 10% of a capacitor's fundamental voltage.

Under the condition of allowable voltage ripples, the minimum capacitance is

$$C_{min} = \frac{V_{dc}(2\pi - 3\theta_3 - \theta_4)}{2\pi f_o \, R_o \, \Delta \, U_{rip}} \quad (13)$$

The inverter needs a smaller capacitor the higher the output frequency f_o and load resistance. However, a bigger capacitor might lessen the voltage ripple. In actuality, a big capacitance will raise the cost and area covered because it is more expensive. As a result, choosing a capacitance involves balancing performance and cost.

E. Analysis of power losses

a. Conduction losses

Conduction losses are the losses brought on by the on-state resistance of power devices and the output voltage drop of diodes. Investigate the three possible operating modes, which include charging and discharging states for both capacitors as well as charging and dissipated states for one capacitor or the other.

The amount of load current during the series parallel connection of capacitors to the corresponding dc voltage sources can be expressed as

$$i_{L,D} = \frac{4V_{dc} + V_{C,1} + V_{C,2}}{5R_{on} + 2r_{ESR} + R_L} \quad (14)$$

Ron, R_D , r_{ESR} , R_L and V_F are internal ON-state resistance of the switch, each diode internal resistance, each capacitor equivalent series resistance (ESR), load resistance and the forward voltage drop incurred in power diode respectively. For a whole cycle of discharging mode, the instantaneous conduction and average conduction loss are therefore determined with respect to time intervals.

$$P_{C,DD} = (5R_{on} + 2r_{ESR}) i_{L,DD}$$

$$\overline{P_{C,DD}} = \frac{2f_{sw}}{\pi}\left(\frac{\pi}{2} - t_8\right) P_{C,DD} \quad (15)$$

The instantaneous and average value of conduction losses for both modes of charging capacitors, taking into account the time provided in the intervals between states of 3 and 5, as well as states of 1 and 2, are provided by

$$\overline{P_{c,cc}} = \frac{2f_{sw}}{\pi}[(t_5 - t_3) + (t_2 - t_1)] P_{c,cc} \quad (16)$$

Hence, V_{Deq} is the each diode voltage drop, and r_{eq} is the power device equivalent resistance. The total conduction power losses are expressed as follows

$$P_{con} = \frac{2}{\pi} \sum_{i=1}^{4} \left[\left(\frac{V_{out} - V_{Deq}}{R_{eq} + R_o}\right) \times r_{eq} \times (\theta_{i+1} - \theta_i)\right] \quad (17)$$

b. Switching loss

The switch on and off processes are lead to switching losses. When a switch's current and voltage are overlapping, switching losses happen throughout the time it takes to get from the ON to the OFF state and vice versa, depending on whether the switch is turned on or off. As a result, these losses are calculable as and are proportional to the fundamental frequency.

$$P_{sw} = (E_{on,s} + E_{off,s}) f_{sw}$$

Where Eon(S) and Eoff(S) are the losses occurred in the switches, and fsw is the frequency of the switch.

The linear approximation of voltage and current can be used to determine the switching losses of the i-th switch.

$$P_{sw,on,i} = f_{sw} \int_0^{t_{on}} V_{sw,i}(t)\, i(t)\, dt$$

$$= \frac{f_{sw} V_{sw} I_i}{6} t_{on} \quad (18)$$

$$P_{sw,off,i} = f_{sw} \int_0^{t_{off}} V_{sw,i}(t)\, i(t)\, dt$$

$$= \frac{f_{sw} V_{sw} I_i}{6} t_{off} \quad (19)$$

where f_{sw} is the i-th switch frequency, V_{sw} is the switching stress voltage, I_i is the i-th switch current, ton is the switch-on time and toff is the switch-off time. The proposed inverter switching loss is

$$P_{sw} = \sum_{i=1}^{11} (P_{sw,on,i} + P_{sw,off,i}) \quad (20)$$

If the proposed topology's switching frequency and voltage stress are low, this can help to lower the inverter's switching loss.

c. Ripple loss

Ripple loss results from the voltage fluctuation of the capacitor. When capacitors are connected in parallel for charging activities, the unwanted losses are caused by the difference between each input voltage and the across voltage of the capacitors. Consequently, the unwanted voltage of the capacitors is obtained from

$$\Delta V_{ci} = \frac{1}{C_i} \int_{t_1}^{t} i_{C1}(t)\, dt \quad (21)$$

The voltage ripple can be calculated by

$$P_{rip} = \frac{V_{dc}(2\pi - 3\theta_3 - \theta_4)}{2\pi f R C}$$

The two capacitors ripple loss of the inverter can be given as

$$P_{rip} = \sum_{k=1}^{2} C_k \Delta U_{rip}^2 f_0 \quad (22)$$

Therefore the proposed inverter ripple loss is

$$P_{rip} = \frac{V_{dc}^2(2\pi - 3\theta_3 - \theta_4)}{2\pi^2 f R^2 C} \quad (23)$$

F. Comparative Study

The topologies used for comparing the different topologies were proposed with the intention of achieving a more number of levels with a high voltage gain while using fewer power devices. In this section, comparisons between the proposed inverter and other MLIs are made to highlight the advantages and disadvantages of each one.

Table: II
Comparison of different inverter topology with proposed topology

Topology	Switch	Diode	Capacitor	Boosting factor	Self balancing	Efficiency	CF
8	8	3	4	1	No	92.8%	29
11	10	4	4	1	Yes	93.5%	36
15	8	3	3	4	Yes	93%	45
23	19	3	3	4	Yes	88.93%	63
Proposed topology	11	0	2	2	Yes	94.8%	36

According to Table's comparison results, both of the inverters suggested in [8] and [11] have the lowest TSV but are unable to increase voltage.

The SCMLI of [15] employs the fewest switches. However, the utilization of diodes and capacitors is increasing. The inverter suggested in [23] contains the most switches, which raises the cost-function (CF) rate.

The SC-based MLI topologies are fairly compared by taking into account each unit TSS per gain. According to the comparison above, the suggested architecture offers the advantages of a single input source, a less device count, capacitor voltage self-balancing, expansion capability, and the capacity to support inductive loads. These benefits enable the inverter's application scope to be increased.

G .Extended Structure of the proposed Inverter

When the load is solely resistive, the Simulink model provides the experimental data of the output voltages and load current.

The output of the inverter voltage and current are unmistakably perfect nine-level stepped waveform, which validates the accuracy of the suggested topology and the viability of the modulation strategy. The experimental waveforms

of output voltages and load current for resistive and inductive loads are shown in the picture below.

It is clear that the output voltage has a typical nine-level stepped waveform, and that the load current is smooth and nearly sine-wavelike. The outcome of the experiment demonstrates the proposed topology's ability to incorporate inductive loads.

The output of inverter voltage of the cascaded based switched capacitor multilevel inverter is increased with reduced components here we use switches, diodes, resistors and capacitors only. The harmonic is also measured by the FFT analysis.

Two capacitors' voltages are constant at or near their rated voltages as soon as the system hits steady state, proving the self-balancing nature of capacitor voltage. Low THD of the suggested inverter attests to its great modulation approach and outstanding structural quality.

III. RESULTS AND DISCUSSION

The given figure gives us an idea about the output voltage, delivered by the multilevel inverter when an input supply of 100V is given to the setup. From the output voltage waveform, it is clearly evident that the proposed inverter setup has the potential to amplify the voltage to the double value of the applied voltage at the source.

The main aim is to generate the pulses accordingly in each and every switch and hence nullify the net error voltage and reduce the total harmonic distortion resulting into a much more efficient total power quality output. The below graph shows the cascaded ninelevel switched capacitor multilevel inverter voltage waveform. The SHE method is used to reduce the harmonics in the multilevel inverter.

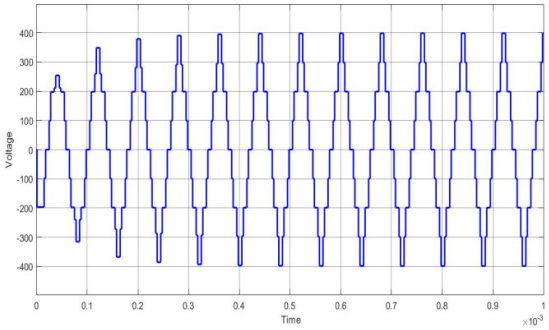

Fig 2. Output voltage waveform of Switched capacitor multilevel inverter

Switching losses are essentially nonexistent when SHE-PWM is taken into account, and conduction losses make up the majority of the overall power losses. The pulses are individually created, provided as input to the switched capacitor units, and then all of the separate units' outputs are added simultaneously to provide the desired output voltage. While capacitor charges, the load voltage is equal to the input voltage (12.5 V), and the output voltage across the capacitor is also equal to the input voltage. The load voltage during dissipating time is the result of adding the input voltage and capacitor voltage, which is 25 V.

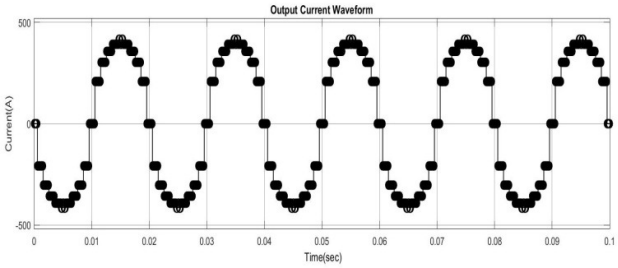

Fig 3. Output Current waveform of switched capacitor multilevel inverter

THD Analysis

Total harmonic distortion causes uneven flow of current through the transmission cables which might cause damage to the appliances so the total harmonic distortion needs to be reduced and the fundamental component has to be achieved. In this 9 level switched capacitor multilevel inverter THD is reduced to 14%.

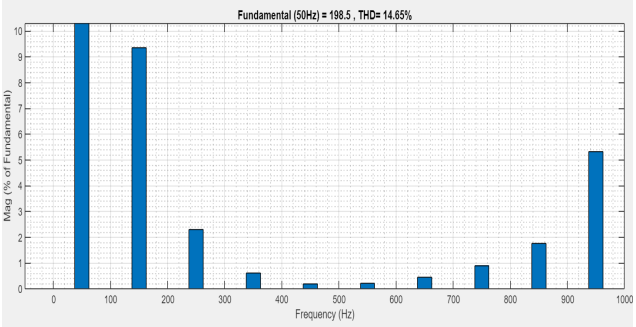

Figure: THD Analysis of switched capacitor multilevel inverter

IV. CONCLUSION

The suggested structure uses fewer components while producing more levels. Without the use of any auxiliary circuits, the capacitor voltage can achieve self-balancing, and the control approach is also streamlined. SHE PWM is used to increase efficiency and lower switching frequency. Additionally, an expanded structure of the suggested topology is suggested with several Switched Capacitor units in order to generate more voltage levels. Analysis has been done on both symmetric and asymmetric instances for choosing the dc source of the inverter. With fewer components, the output of a multilevel inverter based on cascaded switching capacitors was achieved.

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