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INTERLEAVED BOOST FLYBACK CONVERTER

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Abstract

This paper presents a interleaved input current and parallel connection of the output voltage dc-dc converter to achieve high voltage gain. Based on the boost-flyback topology the dc-dc converter was designed. In the proposed converter higher output voltage was obtained. To reduce the input ripple current and output ripple current the interleaved method is used. The boost-flyback converter has high turn-off period compared with a conventional boost converter. To reduce the switching stress the input is connected in parallel and output voltage is connected in series. Finally the simulation is done in the PSIM software and the results are shown.

Keywords : High voltage gain,Boost converter, Flyback converter

NOMENCLATURE

$S_{1,2,3}$ - control switch

$D_{B\ 1,2,3}$ -boost output diode

$D_{F\ 1,2,3}$ -flyback output diode

$C_{F\ 1,2,3}$ -flyback output capacitor

C_D -boost output capacitor

$L_{m\ 1,2,3}$ -magnetising inductor of coupled inductors

$V_{Lm\ 1,2,3}$ -magnetising inductance voltage

$I_{1,2,3}$ -magnetising inductance current in the primary

$I_{4,5,6}$-magnetising inductance current in the secondary

1.INTRODUCTION

The boost-flyback converter is combination of boost and flyback converter[1].The boost converter is mostly used in battery packs for electric automobiles because it has less number of components and its simplicity. Technically, by increasing the duty cycle, the boost converterprovides high output voltage gain. But in practice it is not suitable because the parasitic elements decrease the converter gain. The duty cycle is closed to be unity to obtain high voltage gain[2]. It is not appropriate to implement due to high switch stress and reverse recovery problems.

Another mostly used converter is flyback converter because it provides high voltage gain compared to boost converter. Due to high voltage stress and high current semiconductor stress, the flyback converter is limited to low power applications[3]. In order to reduce the stress the snubber circuits are used but it will increase the losses [4-6]

Input of the circuit is unregulated dc voltage from the utility ac supply after some rectification and filtering. To reduce switching stress interleaved concept is used. The output voltage is connected in series to increase the output voltage. Due to this ripple in input current is reduced, improving reliability and cost is reduced. Due to positive characteristics the boost flyback converter is used in many applications.

The boost-flyback converter is used in power factor correction [7-9], dc-ac[10] and photovoltaic applications[11-13] due to its high efficiency

2.OPERATIONAL STAGES

The proposed converter has eight operational stages of operation shown in Fig.2.1. It consists of four switches, four capacitors, and eight diodes. MOSFET is used as a switch. When the switch is on the primary winding of the transformer is connected to input supply and secondary winding of the transformer is connected to the diode in series. The diode gets reverse bias due to induced voltage. The current carrying is able in the primary winding but in the current in the secondary winding is blocked due to reverse biased switch.

First stage:

In this stage switches S1, S3 and S4 are conduct and switch S2 is blocked, while the diodes DB2 and DF2 are conducting and DB1,DB3,DB4,DF1,DF3 and DF4 are blocked reverse. The capacitor CB and CF2 are charging and CF1,CF3 and CF4 are discharging to provide energy for the load.

Second stage:

The switches s1 and s4 are commanded to conduct and s2 and s3 are blocked. The diodes db2,db3,df2 and df3 are conducting. Thus the capacitors cb, cf2, cf3 are charging and cf1, cf4 are discharging to provide energy for load.

Third Stage:

The switches s1,s2 and s4 are commanded to conduct and s3 is blocked. The diodes db1,db2,db4 and df1,df2 and df4 are conducting. Thus the capacitors cb, cf3 are charging and cf1,cf2 and cf4 are discharging to provide energy for the load.

Fourth Stage:

In fourth stage switch s1 is remain conducting and s2 are commanded to conduct and s3 and s4 are blocked. The diodes db1,db2,df1 and df2 are block reverse and db3,db4,df3 and df4 are conducting. The capacitor cb,cf3 and cf4 are charging and cf1 and cf2 are discharging to provide energy for the load.

Fifth Stage:

In this stage switch s2 and s4 are commanded to conduct and switch s1 and s3 are blocked while the diodes db1,db4,df1 and df4 are conducting and diodes db2,db3,df2 and df3 are blocked reversed. In this way the capacitors cb, cf1 and cf4 are charging and cf2,cf3 are discharging to provide energy for the load.

Sixth Stage:

In this stage switch s2 and s4 are commanded to conduct and switch s1 and s3 are blocked while the diodes db1,db4,df1 and df4 are conducting and diodes db2,db3,df2 and df3 are blocked reversed. In this way the capacitors cb, cf1 and cf4 are charging and cf2,cf3 are discharging to provide energy for the load.

Seventh Stage:

In this stage switch s2 and s4 are commanded to conduct and switch s1 and s3 are blocked while the diodes db1,db4,df1 and df4 are conducting and diodes db2,db3,df2 and df3 are blocked reversed. In this way the capacitors cb, cf1 and cf4 are charging and cf2,cf3 are discharging to provide energy for the load.

The schematic diagram of proposed converter is shown in the figure below.

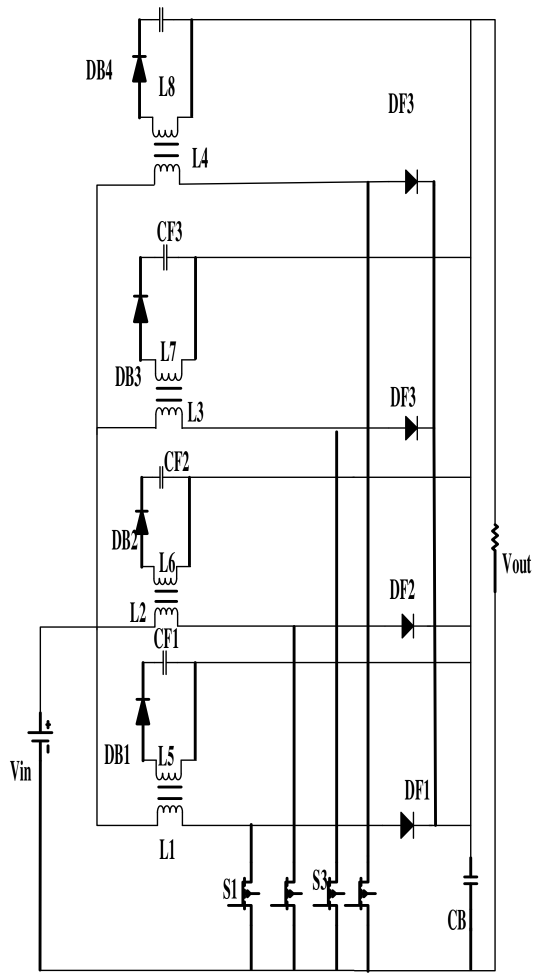

Fig 2.1: Proposed converter

Eight stage:

In this stage switch s2 and s4 are commanded to conduct and switch s1 and s3 are blocked while the diodes db1,db4,df1 and df4 are conducting and diodes db2,db3,df2 and df3 are blocked reversed. In this way the capacitors cb, cf1 and cf4 are charging and cf2,cf3 are discharging to provide energy for the load.

3.MODEL OF PROPOSED CONVERTER

A small signal model is carried out to obtain the transfer function of the proposed converter. The current functions through the switches and voltage functions across the diodes are linearized at the operational point.

$$l\langle I_{s(1,2,3,4)}(t)\rangle_{Ts} = I_{Lm(avg)}(t)d(t)$$
$$\langle V_{DB(1,2,3,4)}(t)\rangle_{Ts} = -V_{CB}(t)\big(1-d(t)\big) \quad (1)$$
$$\langle V_{DF(1,2,3,4)}(t)\rangle_{Ts} = (V_{CB(t)} + nV_{in}(t)(1-d(t))$$

Where

$I_{Lm(avg)}$is the average current through the magnetizing mutual inductance

$V_{CB}$is the boost capacitor output voltage

$V_{in}$is the input voltage

D is the duty cycle

The average large signal model is obtained from(1).

$$\langle I_{s(1,2,3,4)}(t)\rangle_{Ts} = I_{s(1,2,3,4)} + \tilde{\imath}_{s(1,2,3,4)}(t)(2)$$

$$\langle V_{DB(1,2,3,4)}(t)\rangle_{Ts} = V_{DB(1,2,3,4)} + \tilde{V}_{DB(1,2,3,4)}(t)(3)$$

$$\langle V_{DF(1,2,3,4)}(t)\rangle_{Ts} = V_{DF(1,2,3,4)} + \tilde{V}_{DF(1,2,3,4)}(t)(4)$$

$$I_{Lm(1,2,3,4)}(t) = I_{Lm(1,2,3,4)} + \tilde{\imath}_{Lm(1,2,3,4)}(t) \quad (5)$$

$$V_{CF(1,2,3,4)}(t) = V_{CF(1,2,3,4)} + \tilde{v}_{CF(1,2,3,4)}(t) \quad (6)$$

$$V_{CB}(t) = V_{CB} + \tilde{v}_{CB}(t) \quad (7)$$

$$V_{in}(t) = V_{in} + \tilde{v}_{in}(t) \quad (8)$$

$$d(t)_{Ts} = D + \tilde{d}(t) \quad (9)$$

The ac value much smaller than the dc value, it is possible to linearise

$$I_{s(1,2,3,4)} + \tilde{\imath}_{s(1,2,3,4)}(t) = \left[I_{Lm(1,2,3,4)} + \tilde{\imath}_{Lm(1,2,3,4)}(t)\right]\left[D + \tilde{d}(t)\right] \quad (10)$$

Applying the distributive property in (10) and separating the dc terms

$$I_{s(1,2,3,4)} + \tilde{\imath}_{s(1,2,3,4)}(t) = I_{Lm(1,2,3,4)} + \tilde{\imath}_{Lm(1,2,3,4)}(t)D + I_{Lm(1,2,3,4)}\tilde{d}(t) + \tilde{\imath}_{Lm(1,2,3,4)}(t)\tilde{d}(t)$$
(11)

From ac terms separate the dc terms

$$I_{s(1,2,3,4)} = I_{Lm(1,2,3,4)}D(12)$$

$$\tilde{\imath}_{s(1,2,3,4)}(t) = \tilde{\imath}_{Lm(1,2,3,4)}(t)D - \tilde{\imath}_{Lm(1,2,3,4)}(t) \quad (13)$$

Voltage across the diodes

$$\begin{cases} \tilde{v}_{DB}(t) = -\tilde{v}_{CB}(t)D - V_{CB}\tilde{d}(t) \\ \tilde{v}_{DF(1,2,3,4)}(t) = -\tilde{v}_{CB}(t)D - (V_{CB} + nV_{in})\tilde{d}(t) \end{cases} \quad (14)$$

The conventional linear circuit analysis techniques used to solve the linear circuit

Input current transfer function

Applying Laplace transform in the previous equation

$$\begin{gathered} \tilde{\imath}_{s(1,2,3,4)}(t) = \tilde{\imath}_{Lm(1,2,3,4)}(t)D + I_{Lm(1,2,3,4)}\tilde{d}(t) \\ \tilde{v}_{DB}(t) = -\tilde{v}_{CB}(t)D - V_{CB}\tilde{d}(t) \\ \tilde{v}_{DF(1,2,3)}(t) = -\tilde{v}_{CB}(t)D - (V_{CB} + nV_{in})\tilde{d}(t) \\ \tilde{v}_{Lm(1,2,3,4)}(t) = L_{m(1,2,3,4)}\frac{d\tilde{\imath}_{Lm(1,2,3,4)}(t)}{dt} \\ \tilde{v}_{CB}(t) = \frac{1}{C_B}\int \tilde{\imath}_{CB}(t)dt \\ \tilde{v}_{CF(1,2,3,4)}(t) = \frac{1}{C_{F(1,2,3)}}\int \tilde{\imath}_{CF(1,2,3,4)}(t)dt \end{gathered} \quad (15)$$

$$\begin{gathered} \tilde{\imath}_{s(1,2,3,4)}(s) = \tilde{\imath}_{Lm(1,2,3,4)}(s)D + I_{Lm(1,2,3,4)}\tilde{d}(s) \\ \tilde{v}_{DB}(s) = -\tilde{v}_{CB}(s)D - V_{CB}\tilde{d}(s) \\ \tilde{v}_{DF(1,2,3,4)}(s) = -\tilde{v}_{CB}(s)D - (V_{CB} + nV_{in})\tilde{d}(s) \\ \tilde{v}_{Lm(1,2,3,4)}(s) = sL_{m(1,2,3,4)}\tilde{\imath}_{Lm(1,2,3,4)}(s) \\ \tilde{v}_{CB}(s) = \frac{\tilde{\imath}_{CB}(s)}{sC_B} \\ \tilde{v}_{CF(1,2,3,4)}(s) = \frac{\tilde{\imath}_{CF(1,2,3,4)}(s)}{sC_{F(1,2,3,4)}} \end{gathered} \quad (16)$$

Applying Kirchhoff'slaw in

$C_F = C_{F1} = C_{F2} = C_{F3} = C_{F4}andL_m = L_{m1} = L_{m2} = L_{m3} = L_{m4}$

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$$\begin{cases} \tilde{\imath}_{CF(1,2,3,4)}(s) = \\ \frac{s(V_{CF}+nV_{in})C_F\tilde{d}(s)}{1-D} - \frac{\tilde{\imath}_{Lm(1,2,3,4)}(s)s^2nL_mC_F}{1-D} \\ \tilde{\imath}_{CB}(s) = \frac{s(V_{CB}C_B)\tilde{d}(s)}{1-D} - \frac{\tilde{\imath}_{Lm(1,2,3,4)}(s)s^2nL_mC_B}{1-D} \\ \tilde{\imath}_0(s) = \frac{\tilde{\imath}_{CB}(s)}{sC_BR_0} + \frac{3\tilde{\imath}_{CF(1,2,3,4)}(s)}{sC_FR_0} \\ \tilde{\imath}_{(5,6,7,8)}(s) = \tilde{\imath}_{CF(1,2,3,4)}(s) + \tilde{\imath}_0(s) \\ \tilde{\imath}_{in}(s) = 3\tilde{\imath}_{(1,2,3,4)}(s) = \tilde{\imath}_{Lm(1,2,3)}(s) \\ -n\tilde{\imath}_4(s)3\tilde{\imath}_{Lm(1,2,3,4)}(s)\tilde{d}(s) + \tilde{\imath}_{CB}(s) \end{cases} \quad (17)$$

To obtain input current transfer function solving the equation

Output voltage transfer function

To obtain output current the equation (17) must be solved

$$FT_{v_{out}}(s) = \frac{\tilde{v}_{out}(s)}{\tilde{d}(s)} = \frac{c+cs_1+c_0}{d_2s^2+d_1s+d_0} \quad (18)$$

4.Experimental results

Thus the Fig.4.1 shows that the proposed converter provides good efficiency when compared to other conventional converter.

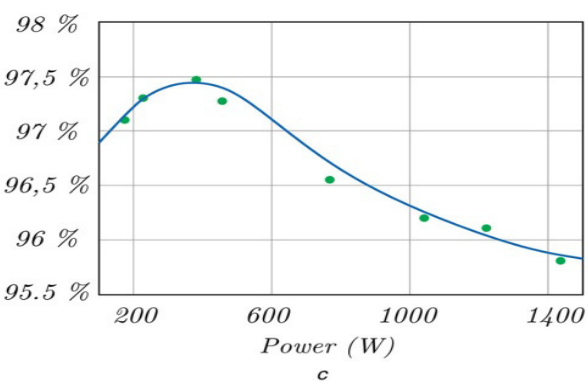

Fig.4.1: Efficiency curve

To evaluate the proposed converter efficiency, tests were carried out varying the power from 0 up to 1.5 kW, as shown in the figure 4.1.Note that, for all the power range, the topology presents high efficiency, reaching 97.5% when the converter operates with 400 W.

The current waveform through the diode and switch is shown in the figure 4.2 and figure 4.3 respectively.

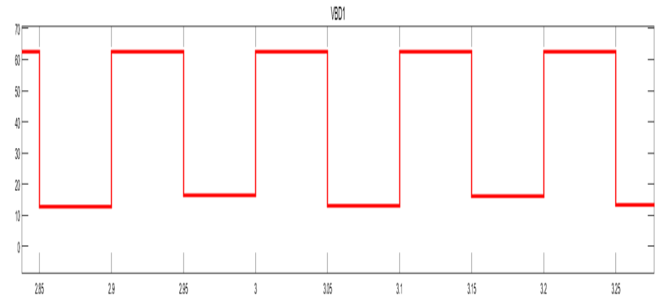

Fig.4.2: Diode current waveform

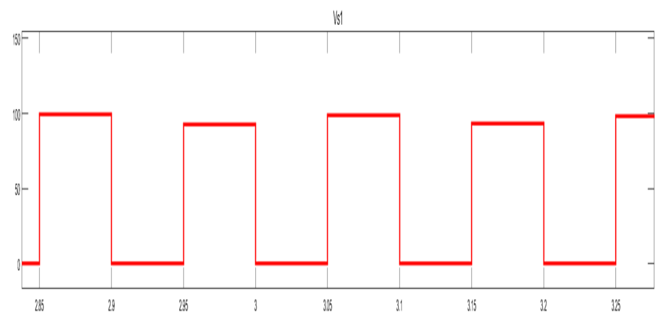

Fig.4.3: Diode current waveform

5.PERFORMANCE COMPARISION

The performance of the proposed converter is compared with other topologies is shown in Table 1.

Table 1. Comparison of similar prototypes

	Converter [14]	Converter [15]	Proposed converter
Quantities of switches	2	2	4
Quantities of diodes	6	4	8
Quantities of cores	2	3	4
Quantities of capacitor	5	3	5
Maximum efficiency	95.8	95.8	98
Voltage stress on the active switch	Vout/(2n+2)	Vout/(2+n D(1-D))	Vout/(1+n D)
Voltage stress on diodes	nVout/(n+1)	2Vout/(2+n D(1-D))	Vout/(1+n D)

From this table, It is clear that the voltage stress across the diode in the proposed converter is very less when compared to other converter. There is an increase in efficiency is also seen in this proposed model.

6.CONCLUSION

A high gain dc-dc converter was designed based boost-flyback topology with the input current is interleaved in the input stage and output voltage is connected in series .The interleaved techniques reduce the ripple in the input current. It is used in EV applications where due to reduced ripple. To increase the life span the EV battery requires high current values and low ripple current.

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