RESEARCHARTICLE OPENACCESS

AREA-DELAY AND ENERGY EFFICIENT MULTI OPERAND BINARY TREE ADDER

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ABSTRACT:

In this project, a binary based n-bit operand RCA is proposed using some new logic formulation for carry generation. In general, the critical path of the ripple carry adder (RCA)-based binary tree adder (BTA) is analysed to find the possibilities for delay minimization. To reduce the delay new logic formulation and the corresponding design of RCA are proposed for the BTA. The result shows that the proposed RCA design offers better efficiency in terms of area, delay and energy than the existing RCA. Using this RCA design, the BTA structure is proposed. The synthesis result shows the performance of multiplier designs improve significantly due to the use of proposed logic formulation. Therefore, the proposed BTA design can be a better choice to develop the area, delay and energy efficient digital systems for signal and image processing applications. The effectiveness of the proposed method is synthesized and simulated using XilinxISE14.7.

Keywords **—Binary Tree Adder, Ripple Carry Adder, AOI, OAI, Multi operand adder.**

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I. INTRODUCTION

Themulti-operandadders(MOAs)arewidelyused in the modern low-power and high-speed portable very-large-scale integration systems for image and signal processing applications such as digital filters, transforms by connecting two-operand adders in binary tree configuration for the addition ofmultiple operands.

The simplest MOA is a binary tree adderdesigned by connecting two operand adders in binary tree configuration for the addition of multiple operands.

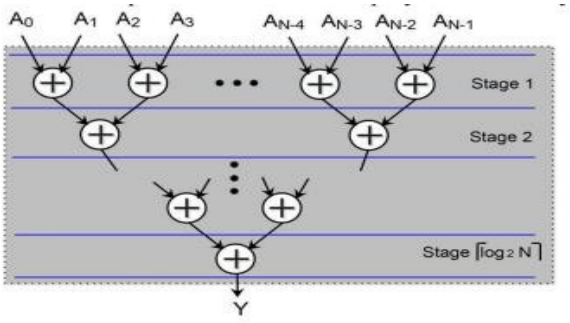

Fig 1: Generalised N-operand BTA structure

To achieve optimal system performance while maintaining physical security, it is necessary to implement cryptography algorithms on hardware.

Modular arithmetic such as modular exponentiation, modular multiplication and modular addition is frequently used for the arithmetic operations in various cryptography algorithms.

II.RELATED WORK

In the previous project, the four-operand RCA-BTA structure is considered for the delay analysis. It produces sum(Y) of four operands (A0, A1, A2 and A3) using three RCAs, where each operand is of 4 bits. From (1), it seems that each addition stage introduces one RCA delay while from the delay analysis mentioned in fig. 2, it is found that the first leveladditiontakesone4-bitRCAdelaywhereasthe second level requires only two FA delays instead of a 5-bit RCA delay.

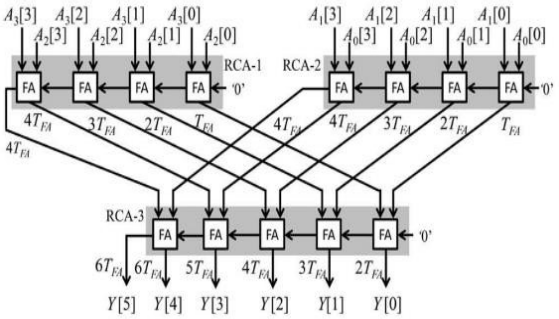

Fig 2: RCA based four operand BTA

III.METHODOLOGY

The total progress of the process which are done in this methodology by using the apparatus which are used their process also explained clearly.

A.AOI GATE AND OAI GATES

AND-AR-invert (AOI) logic and AOI gates are two-level compound (or complex) logic function constructed from the combination of one or more AND gates followed by a NOR gate. Construction of AOI cells is particularly efficient using CMOS technology where the total number of transistor gates can be compared to the same construction using NAND logic or NOR logic.

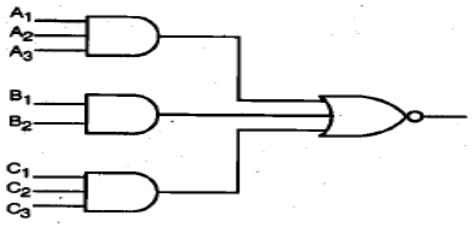

Fig 3: AOI gate

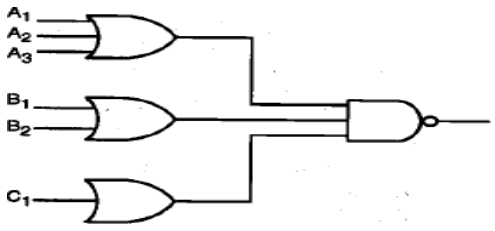

Fig 4: OAI gate

AND-OR-INVERT (AOI) and OAI gates can be readily implemented in CMOS circuitry. AOI gates are particularly advantaged in that the total number of transistors (orgates) is less than if the AND,NOT, and OR functions were implemented separately. This results in increased speed, reduced power, smaller area, and potentially lower fabrication cost. For example, a 2-1 AOI gate can be constructed with 6 transistors in CMOS compared to 10 transistors using a 2-input NAND gate (4 transistors), an inverter (2 transistors), and a 2-input NOR gate (4 transistors).

Furture, anew logic formation is used to derive the RCA design. Subsequently, the BTA structure is proposed using this RCA design. The new logic formulation for RCA is proposed,which supports the

complementary gate-based realization. Further, this formation is used to develop the RCA design.

B. FULL ADDER

Full adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C. The output carry is designated as CARRY and the normal output is designated as SUM.

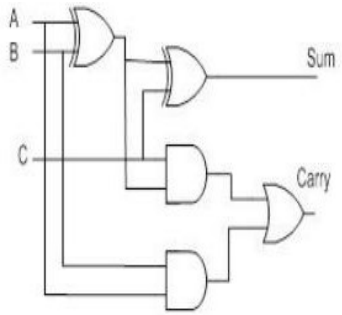

Fig 5: Full adder

Multiple bit addition can be obtained by using a number of full adders and connection them as required for proper carry propagation. Ripple carry adder is the simplest and the most common type of multiple bit adder circuit. It requires as many full adder circuits as the number of bits to be added. Carry is propagated from the LSB to MSB which cause the maximum delay as compared too ther more efficient adders. Universal gates are used to design a simple half adder circuit. Two half adder circuits and an OR logic can be cascaded to form a ripple carry adder.

C. RIPPLE CARRY ADDER

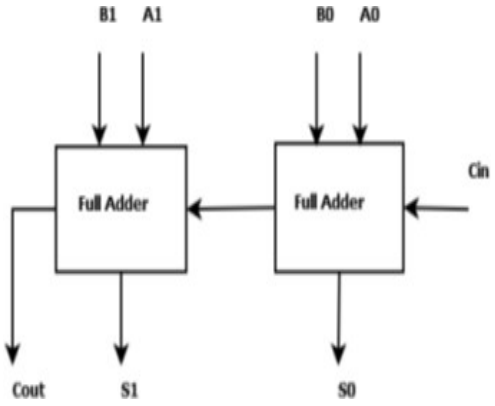

Fig 6: 2 bit RCA

A full adder can be implemented using a half adder by cascading the two half adders. In the similar way two bit adder can formed by cascading the two full adders. To get n bit adder n full adders are cascaded which we can refer as a ripple carry adder.

In doing so,the designers often trade off o the vital requirements such as driving capability, noise immunity, and area. Their performance as a single unit is good but when large adders are built by cascadingthese1-bfulladdercells,the performance degrades drastically. At the circuit level, an optimized design is desired to avoid any degradation in the output voltage, low power consumption, reduced delay in critical path.

D.BINARY TREEADDER

The are a, delay and energy efficiency of the BTA depends on the performance of adders used in the structure. The simplest MOA is a binary tree adder (BTA), designed by connecting two-operand adders in binary tree configuration for the addition of multiple operands.

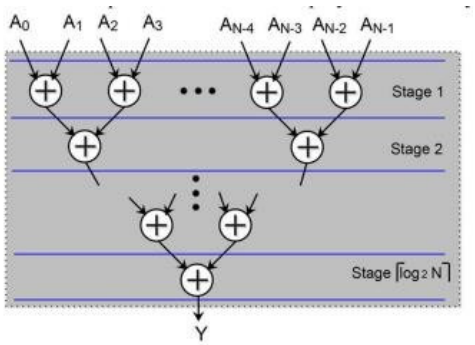

Fig 7: Binary tree adder

IV. OVERVIEW OF THE PROPOSED WORK

The proposed BTA structure for N = 8 and m = 4 is shown in Fig. below. It consists of seven RCAs, where the first stage uses four 4- bit RCAs, the secondstageusestwo5-bitRCAsandthethirdstage uses one 6-bit RCA. These RCAs are made from AOI-LC and OAI-LC modules. The proposed BTA structure is scalable for any values of N andm.

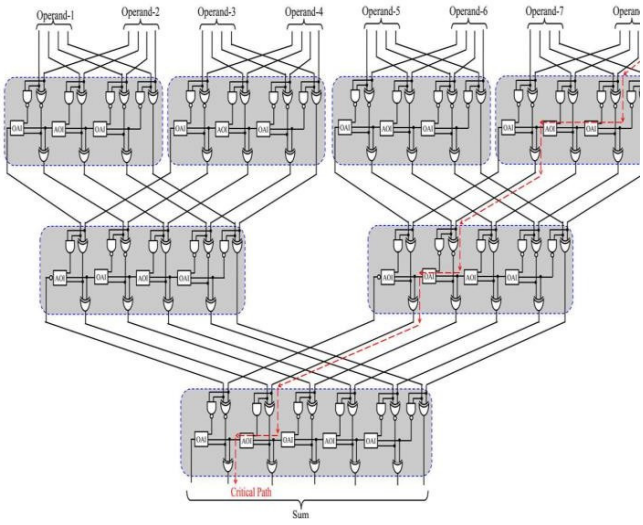

Fig 8 : Proposed BTA structure for eight 4 bit operands

The first, second and third addition stages of the proposed BTA, respectively, introduced four gates (one XNOR, one OAI, one AOI and one XOR),three gates (one XNOR, one OAI and one XOR) and three gates (one AOI and two XOR) in the critical path which is shown with red dotted line. For simplicity in delay estimation, the equal delay is considered for AOI and OAI gates, similarly equal delay for XOR and XNOR gates.

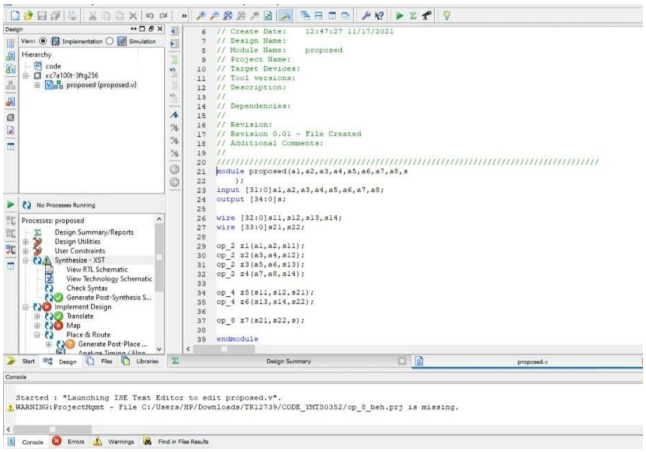

Fig 9:code explanation for proposed method

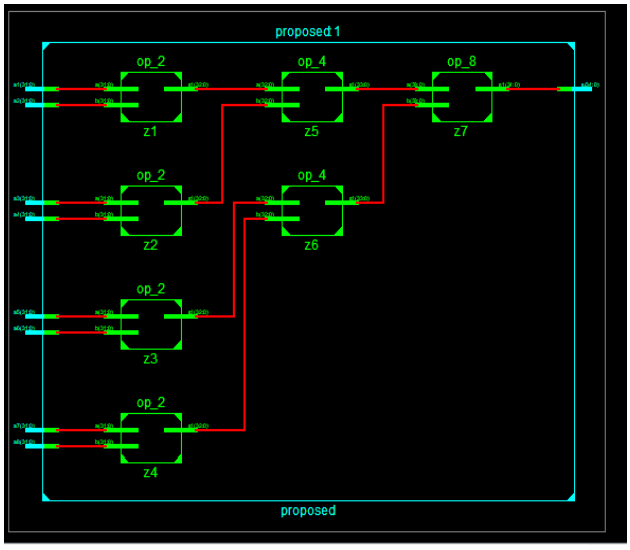

Fig 10: RTL schematic

RTL is a register transfer logic and technology schematic shows the connection of wires internally.

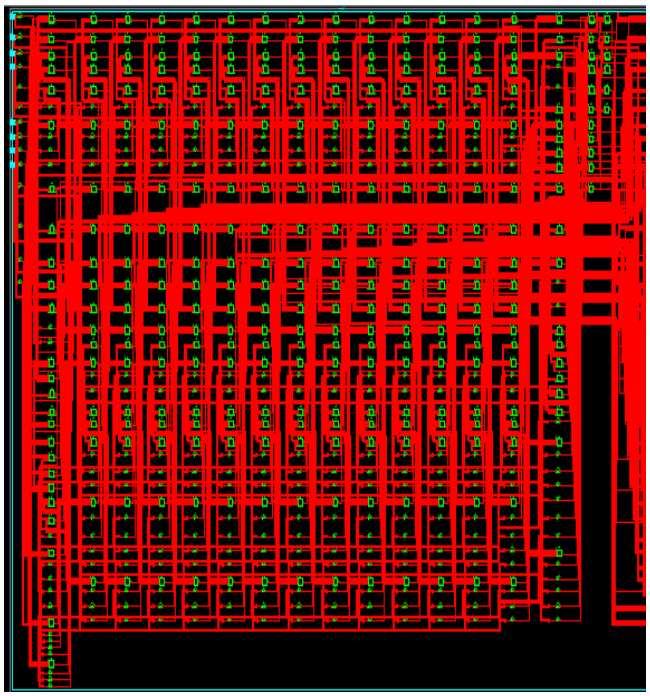

Fig11: Technology schematic

The simulation widow will appear pass the inputvalues by making force constant and if it is clock by making force clock. By Mentioning the simulation period and run for certain time and results will appear as shown in following window.

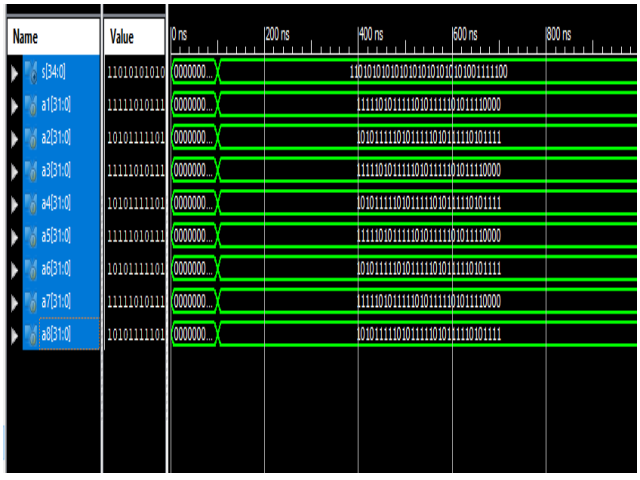

Fig 12: Simulation results

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Device utilization summary:
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Selected Device : 7a100tftg256-3


Slice Logic Utilization:
 Number of Slice LUTs:                  343  out of  63400     0%
    Number used as Logic:               343  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    343
   Number with an unused Flip Flop:     343  out of    343   100%
   Number with an unused LUT:             0  out of    343     0%
   Number of fully used LUT-FF pairs:     0  out of    343     0%
   Number of unique control sets:         0
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Fig13: Area report

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Timing Details:
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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
  Total number of paths / destination ports: 583774 / 35
---------------------------------------------------------
Delay:               10.343ns (Levels of Logic = 21)
  Source:            a1<1> (PAD)
  Destination:       s<34> (PAD)
```

Fig14: Delay report

EVALUATION TABLE:

	Area(LUT's)	Delay(ns)
Proposed	343	10.343

Table no.:01

V.CONCLUSION

In this paper, an efficient approach for designing reversible ripple carry adder and carry look-ahead adder has been proposed. The designs imply that their outputs contain as much information as their inputs they can operate with arbitrarily low dissipation. These adders can be used further as an indispensable part of future development on Quantum computers. The proposed design is optimized in terms of delay and hardware complexity. Firstly, the gate used here, in carry look ahead adder are parity preserving gates, hence the whole adder preserves the parity. Therefore, no intermediate checking will be required if there is no fault detected. Secondly, the circuitry for reversible ripple carry adder generates less complexities and delays, hence proving to be a valuable asset in being an integral part of the Quantum computer blocks. By integrating the proposed design parallel processing in adding the input has been achieved.

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